PENTEK®
Setting the Standard for Digital Signal Processing

Software-Defined Radio Handbook

11th Edition

Sampling

Principles of SDR

Technology

Products

Applications

by

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Preface

SDR (Software-Defined Radio) has revolutionized electronic systems for a variety of applications including communications, data acquisition and signal processing.

This handbook shows how DDCs (Digital Downconverters) and DUCs (Digital Upconverters), the fundamental building blocks of SDR, can replace legacy analog receiver and transmitter designs while offering significant benefits in performance, density and cost.

In order to fully appreciate the benefits of SDR, conventional analog receiver and transmitter systems will be compared to their digital counterparts, highlighting similarities and differences.

The inner workings of the SDR will be explored with an in-depth description of the internal structure and the devices used. Finally, some actual board- and system-level implementations and available off-the-shelf SDR products and applications based on such products will be presented.

For more information on complementary subjects, the reader is referred to these Pentek Handbooks:

Putting FPGAs to Work in Software Radio Systems

Critical Techniques for High-Speed A/D Converters in Real-Time Systems

High-Speed Switched Serial Fabrics Improve System Design

High-Speed, Real-Time Recording Systems

Sampling

Nyquist's Theorem and Sampling

Before we look at SDR and its various implementations in embedded systems, we'll review a theorem fundamental to sampled data systems such as those encountered in Software-Defined Radios.

Nyquist's Theorem:

"Any signal can be represented by discrete samples if the sampling frequency is at least twice the bandwidth of the signal."

Notice that we highlighted the word bandwidth rather than frequency. In what follows, we'll attempt to show the implications of this theorem and the correct interpretation of sampling frequency, also known as sampling rate.

A Simple Technique to Visualize Sampling

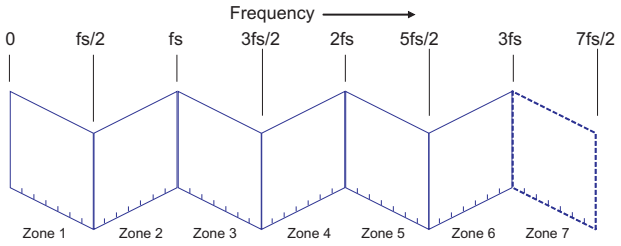

Figure 1

To visualize what happens in sampling, imagine that you are using transparent "fan-fold" computer paper. Use the horizontal edge of the paper as the frequency axis and scale it so that the paper folds line up with integer multiples of one-half of the sampling frequency f_s. Each sheet of paper now represent what we will call a "Nyquist Zone", as shown in Figure 1.

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Sampling

Sampling Basics

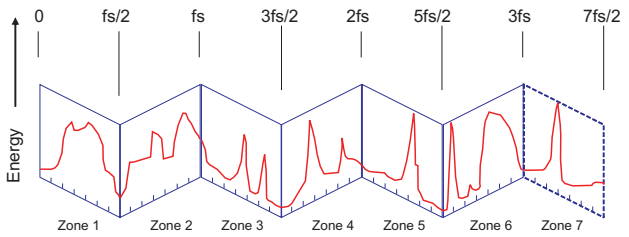

Figure 2

Use the vertical axis of the fan-fold paper for signal energy and plot the frequency spectrum of the signal to be sampled, as shown in Figure 2. To see the effects of sampling, collapse the transparent fan-fold paper into a stack.

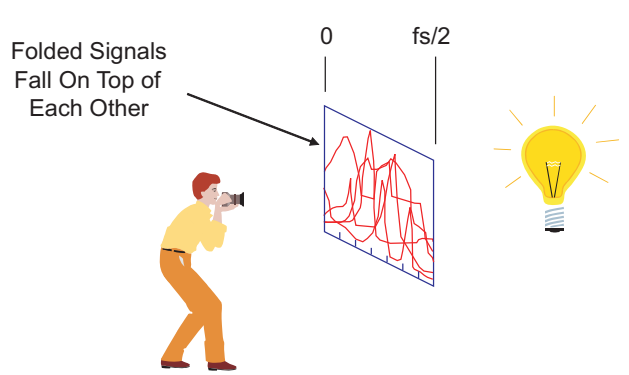

Figure 3

The resulting spectrum can be seen by holding the transparent stack up to a light and looking through it. You can see that signals on all of the sheets or zones are "folded" or "aliased" on top of each other — and they can no longer be separated.

Once this folding or aliasing occurs during sampling, the resulting sampled data is corrupted and can never be recovered. The term "aliasing" is appropriate because after sampling, a signal from one of the higher zones now appears to be at a different frequency.

Baseband Sampling

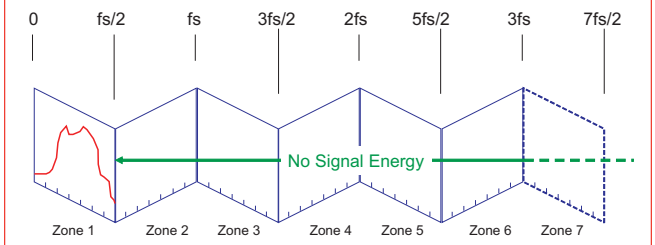

Figure 4

A baseband signal has frequency components that start at $f = 0$ and extend up to some maximum frequency.

To prevent data destruction when sampling a baseband signal, make sure that all the signal energy falls ONLY in the 1st Nyquist band, as shown in Figure 4.

There are two ways to do this:

1. Insert a lowpass filter to eliminate all signals above $f_s/2$, or
2. Increase the sampling frequency so all signals present fall below $f_s/2$.

Note that $f_s/2$ is also known as the "folding frequency".

Sampling Bandpass Signals

Let's consider bandpass signals like the IF frequency of a communications receiver that might have a 70 MHz center frequency and 10 MHz bandwidth. In this case, the IF signal contains signal energery from 65 to 75 MHz.

If we follow the baseband sampling rules above, we must sample this signal at twice the highest signal frequency, meaning a sample rate of at least 150 MHz.

However, by taking advantage of a technique called "undersampling", we can use a much lower sampling rate.

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Undersampling

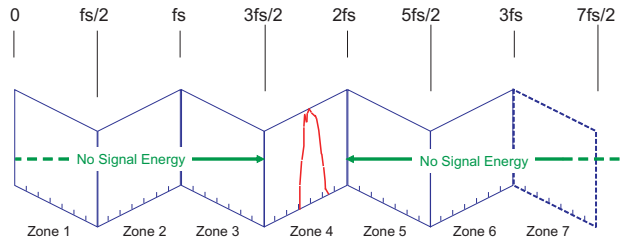


Figure 5

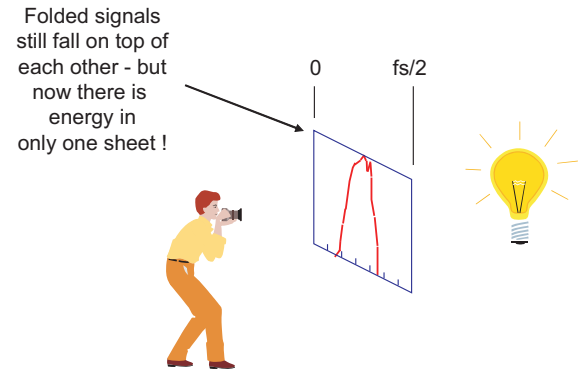


Figure 6

Undersampling allows us to use aliasing to our advantage, providing we follow the strict rules of the Nyquist Theorem.

In our previous IF signal example, suppose we try a sampling rate of 40 MHz.

Figure 5 shows a fan-fold paper plot with Fs = 40 MHz. You can see that zone 4 extends from 60 MHz to 80 MHz, nicely containing the entire IF signal band of 65 to 75 MHz.

Now when you collapse the fan fold sheets as shown in Figure 6, you can see that the IF signal is preserved after sampling because we have no signal energy in any other zone.

Also note that the odd zones fold with the lower frequency at the left (normal spectrum) and the even zones fold with the lower frequency at the right (reversed spectrum).

In this case, the signals from zone 4 are frequency-reversed. This is usually very easy to accommodate in the following stages of SDR systems.

The major rule to follow for successful undersampling is to make sure all of the energy falls entirely in one Nyquist zone.

There two ways to do this:

1. Insert a bandpass filter to eliminate all signals outside the one Nyquist zone.
2. Increase the sampling frequency so all signals fall entirely within one Nyquist zone.

Summary

Baseband sampling requires the sample frequency to be at least twice the signal bandwidth. This is the same as saying that all of the signals fall within the first Nyquist zone.

In real life, a good rule of thumb is to use the 80% relationship:

$$\text{Bandwidth} = 0.8 * f_s / 2 = 0.4 * f_s$$

Undersampling allows a lower sample rate even though signal frequencies are high, PROVIDED all of the signal energy falls within one Nyquist zone.

To repeat the Nyquist theorem: The sampling frequency must be at least twice the signal bandwidth — not the signal frequency.

Analog Radio Receiver Block Diagram

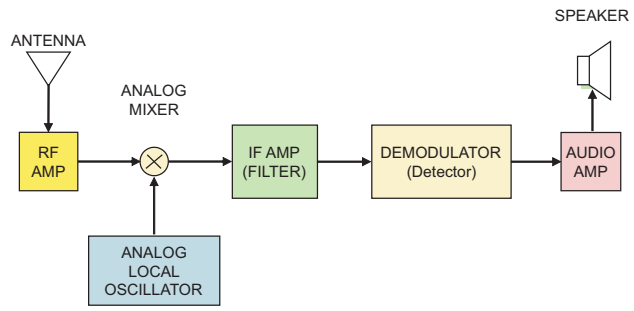


Figure 7

Analog Radio Receiver Mixer

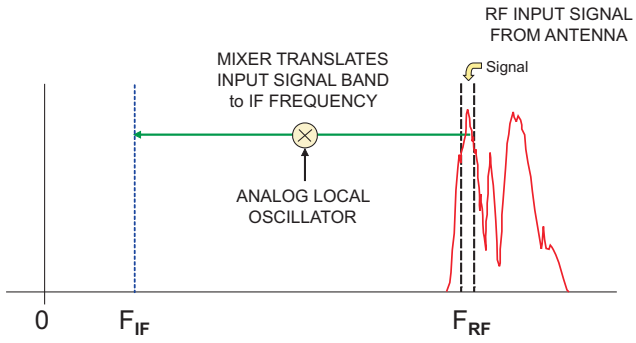


Figure 8

The conventional heterodyne radio receiver shown in Figure 7, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to a digital receiver becomes apparent.

First the RF signal from the antenna is amplified, typically with a tuned RF stage that amplifies a region of the frequency band of interest.

This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is determined by the tuning control of the radio.

The mixer translates the desired input signal to the IF (Intermediate Frequency) as shown in Figure 8.

The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts.

The demodulator recovers the original modulating signal from the IF output using one of several different schemes.

For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio power amplifier which drives a speaker.

The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and the desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to:

$$100.7 - 10.7 = 90 \text{ MHz}$$

This is called "downconversion" or "translation" because a signal at a high frequency is shifted down to a lower frequency by the mixer.

The IF stage acts as a narrowband filter which only passes a "slice" of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the "radio station") that you are trying to receive.

For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

SDR Receiver Block Diagram

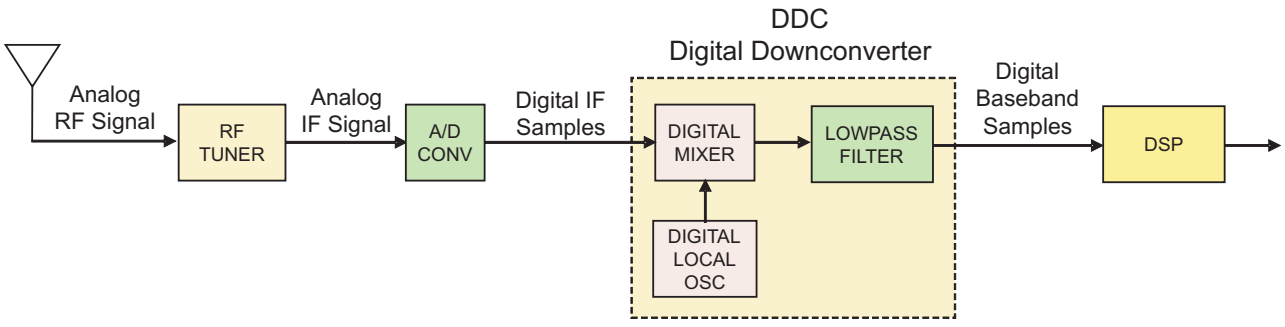


Figure 9

Figure 9 shows a block diagram of a software defined radio receiver. The RF tuner converts analog RF signals to analog IF frequencies, the same as the first three stages of the analog receiver.

The A/D converter that follows digitizes the IF signal thereby converting it into digital samples. These samples are fed to the next stage which is the digital downconverter (DDC) shown within the dotted lines.

The digital downconverter is typically a single monolithic chip or FPGA IP, and it is a key part of the SDR system.

A conventional DDC has three major sections:

- **A digital mixer**
- **A digital local oscillator**
- **An FIR lowpass filter**

The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR lowpass filter limits the signal bandwidth and acts as a decimating lowpass filter. The digital downconverter includes a lot of hardware multipliers, adders and shift register memories to get the job done.

The digital baseband samples are then fed to a block labeled DSP which performs tasks such as demodulation, decoding and other processing tasks.

Traditionally, these needs have been handled with dedicated application-specific ICs (ASICs), and programmable DSPs.

SDR Receiver Mixer

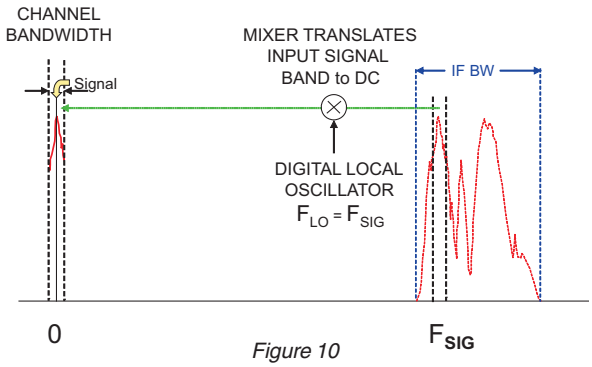


Figure 10

At the output of the mixer, the high frequency wideband signals from the A/D input (shown in Figure 10 above) have been translated down to DC as complex I and Q components with a frequency shift equal to the local oscillator frequency.

This is similar to the analog receiver mixer except *there*, the mixing was done down to an IF frequency. *Here*, the complex representation of the signal allows us to go right down to DC.

By tuning the local oscillator over its range, any portion of the RF input signal can be mixed down to DC.

In effect, the wideband RF signal spectrum can be "slid" around 0 Hz, left and right, simply by tuning the local oscillator. Note that upper and lower sidebands are preserved.

DDC Local Oscillator and Decimation

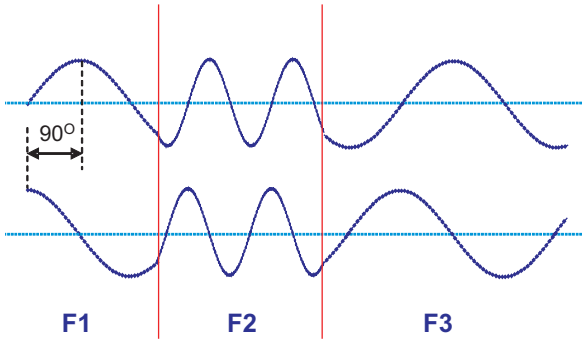


Figure 11A Local Oscillator Frequency Switching

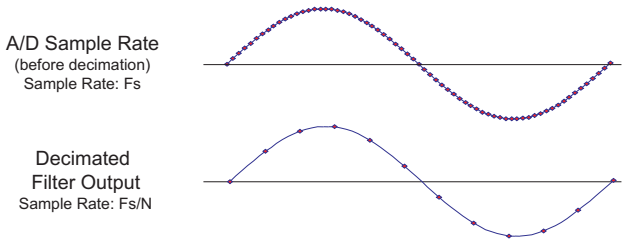


Figure 11B FIR Filter Decimation

Because the local oscillator uses a digital phase accumulator, it has some very nice features. It switches between frequencies with phase continuity, so you can generate FSK signals or sweeps very precisely with no transients as shown in Figure 11A.

The frequency accuracy and stability are determined entirely by the A/D clock so it's inherently synchronous to the sampling frequency. There is no aging, drift or calibration since it's implemented entirely with digital logic.

Since the output of the FIR filter is band-limited, the Nyquist theorem allows us to lower the sample rate. If we are keeping only one out of every N samples, as shown in Figure 11B above, we have dropped the sampling rate by a factor of N.

DDC Signal Processing

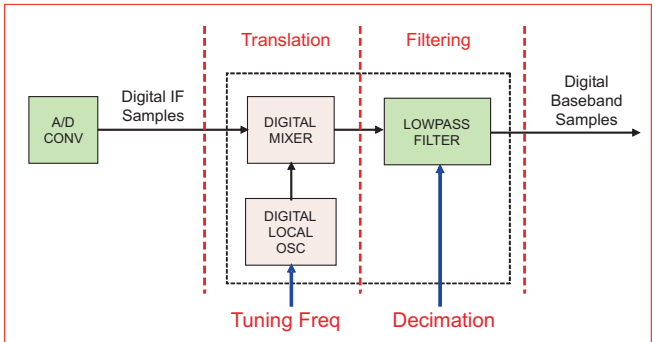


Figure 12

This process is called *decimation* and it means keeping one out of every N signal samples. If the decimated output sample rate is kept higher than twice the output bandwidth, no information is lost.

The clear benefit is that decimated signals can be processed easier, can be transmitted at a lower rate, or stored in less memory. As a result, decimation can dramatically reduce system costs!

As shown in Figure 12, the DDC performs two signal processing operations:

1. Frequency translation with the tuning controlled by the local oscillator.
2. Lowpass filtering with the bandwidth controlled by the decimation setting.

We will next turn our attention to the Software-Defined Radio Transmitter.

SDR Transmitter Block Diagram

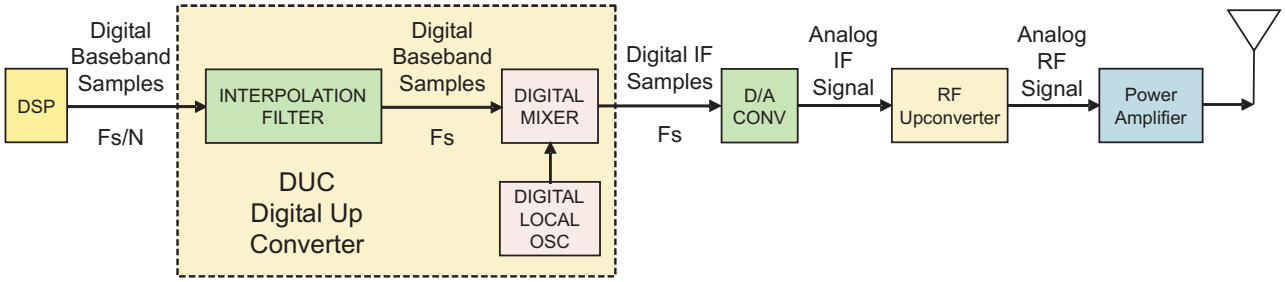


Figure 13

The input to the transmit side of an SDR system is a digital baseband signal, typically generated by a DSP stage as shown in Figure 13 above.

The digital hardware block in the dotted lines is a DUC (digital upconverter) that translates the baseband signal to the IF frequency.

The D/A converter that follows converts the digital IF samples into the analog IF signal.

Next, the RF upconverter converts the analog IF signal to RF frequencies.

Finally, the power amplifier boosts signal energy to the antenna.

DUC Signal Processing

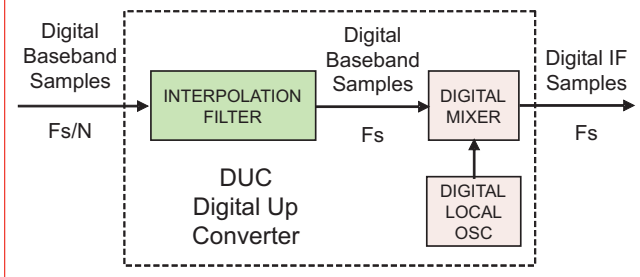


Figure 14

Inside the DUC shown in Figure 14, the digital mixer and local oscillator at the right translate baseband samples up to the IF frequency. The IF translation frequency is determined by the local oscillator.

The mixer generates one output sample for each of its two input samples. And, the sample frequency at the mixer output must be equal to the D/A sample frequency f_s.

Therefore, the local oscillator sample rate and the baseband sample rate must be equal to the D/A sample frequency f_s.

The local oscillator already operates at a sample rate of f_s, but the input baseband sample frequency at the left is usually much lower. This problem is solved with the *Interpolation Filter.*

Interpolation Filter: Time domain

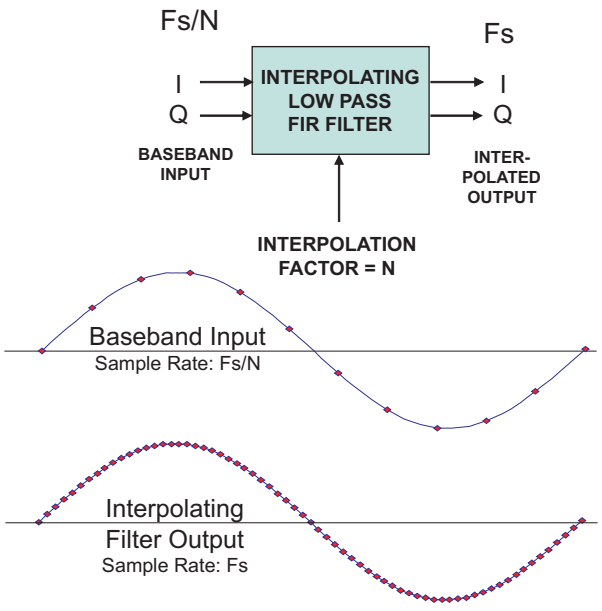


Figure 15

Interpolation Filter: Frequency Domain

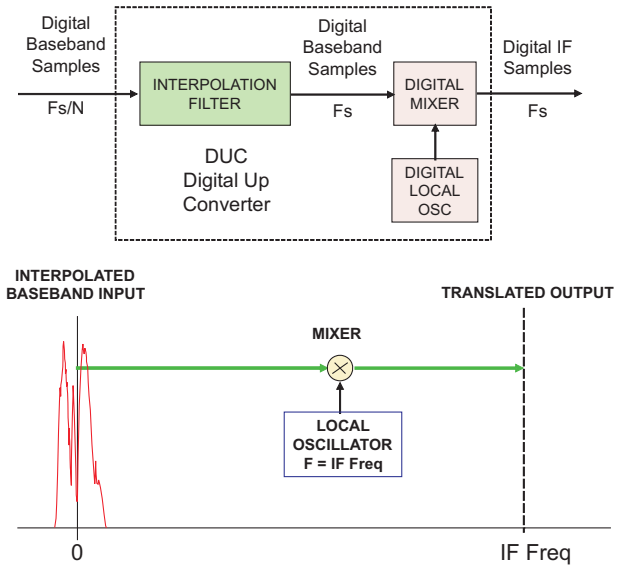


Figure 16

The interpolation filter must boost the baseband input sample frequency of f_s / N up to the required mixer input and D/A output sample frequency of f_s.

The interpolation filter increases the sample frequency of the baseband input signal by a factor N, known as the interpolation factor.

At the bottom of Figure 15, the effect of the interpolation filter is shown in the time domain.

Notice the baseband signal frequency content is completely preserved by filling in additional samples in the spaces between the original input samples.

The signal processing operation performed by the interpolation filter is the inverse of the decimation filter we discussed previously in the DDC section.

Figure 16 is a frequency domain view of the digital upconversion process.

This is exactly the opposite of the frequency domain view of the DDC in Figure 10.

The local oscillator setting is set equal to the required IF signal frequency, just as with the DDC.

DDC Processing

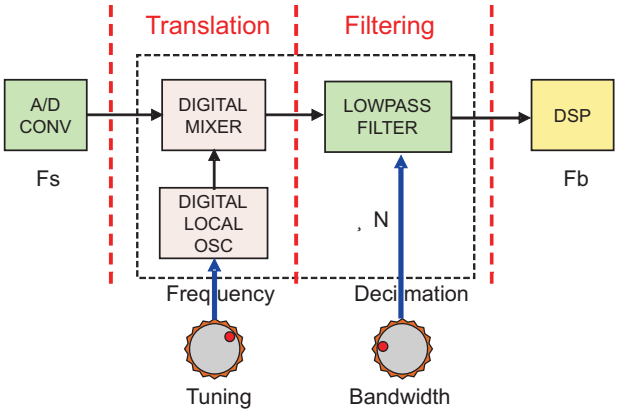


Figure 17

Figure 17 shows the two-step processing performed by the digital downconverter.

Frequency translation from IF down to baseband is performed by the local oscillator and mixer.

The "tuning knob" represents the programmability of the local oscillator frequency to select the desired signal for downconversion to baseband.

The baseband signal bandwidth is set by setting decimation factor N and the lowpass FIR filter:

- Baseband sample frequency $f_b = f_s / N$
- Baseband bandwidth = $0.8 * f_b$

The baseband bandwidth equation reflects a typical 80% passband characteristic, and complex (I+Q) samples.

The "bandwidth knob" represents the programmability of the decimation factor to select the desired baseband signal bandwidth.

DUC Processing

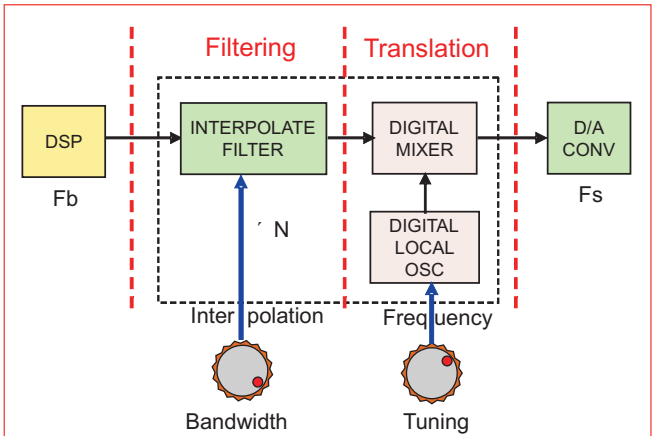


Figure 18

Figure 18 shows the two-step processing performed by the digital upconverter:

The ratio between the required output sample rate and the sample rate input baseband sample rate determines the interpolation factor N.

- Baseband bandwidth = $0.8 * f_b$
- Output sample frequency $f_s = f_b * N$

Again, the bandwidth equation assumes a complex (I+Q) baseband input and an 80% filter.

The "bandwidth knob" represents the programmability of the interpolation factor to select the desired input baseband signal bandwidth.

Frequency translation from baseband up to IF is performed by the local oscillator and mixer.

The "tuning knob" represents the programmability of the local oscillator frequency to select the desired IF frequency for translation up from baseband.

Key DDC and DUC Benefits

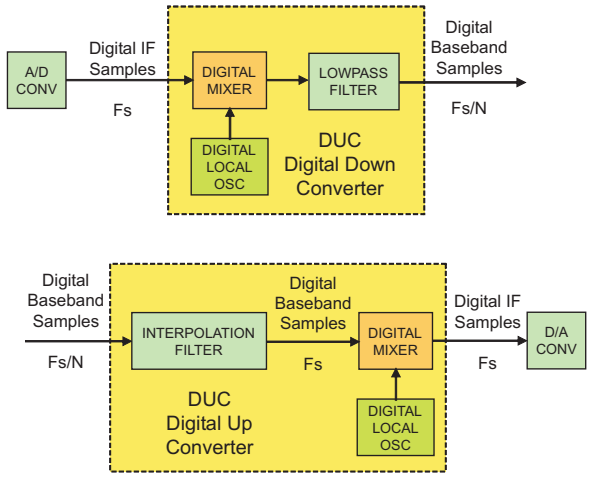


Figure 19

SDR Tasks

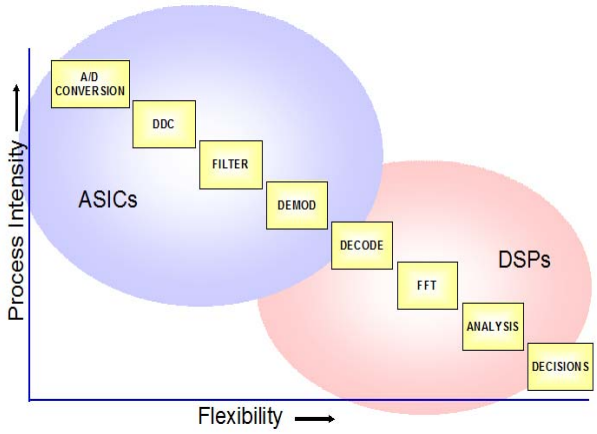


Figure 20

Think of the DDC as a hardware preprocessor for programmable DSP or GPP processor. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the processor.

The same applies to the DUC. The processor only needs to generate and deliver the baseband signals sampled at the baseband sample rate. The DUC then boosts the sampling rate in the interpolation filter, performs digital frequency translation, and delivers samples to the D/A at a very high sample rate.

The number of processors required in a system is directly proportional to the sampling frequency of input and output data. As a result, by reducing the sampling frequency, you can dramatically reduce the cost and complexity of the programmable DSPs or GPPs in your system.

Not only do DDCs and DUCs reduce the processor workload, the reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem. This helps minimize recording time and disk space, and reduces traffic and bandwidth across communication channels.

Here we've ranked some of the popular signal processing tasks associated with SDR systems on a two axis graph, with computational Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left, are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs are usually chosen for these functions.

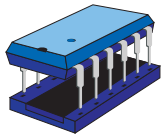
Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision making which are highly variable and often subjective.

Programmable general-purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let's temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
  - Control logic
  - Glue logic
  - Registers and gates
  - State machines
  - Counters and dividers



- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

Figure 21

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
  - Schematic processors
  - Boolean processors
  - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
  - Critical paths and propagation delays
  - Pin assignment and pin locking
  - Signal loading and drive capabilities
  - Clock distribution
  - Input signal synchronization and skew analysis

Figure 22

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

FPGAs: New Device Technology

- 500+ MHz DSP slices and memory structures
- Over 3500 dedicated on-chip hardware multipliers
- On-board GHz serial transceivers
- Partial reconfigurability maintains operation during changes
- Switched fabric interface engines
- Over 690,000 logic cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC microcontroller cores
- Memory densities approaching 85 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 28 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards

Figure 23

FPGAs: New Development Tools

- High Level Design Tools
  - Block Diagram System Generators
  - Schematic Processors
  - High-level language compilers for VHDL & Verilog
  - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - Faster compilers and simulators save time
  - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
  - FPGA vendors offer both free and licensed cores
  - FPGA vendors promote third party core vendors
  - Wide range of IP cores available

Figure 24

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you'll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from steadily shrinking silicon geometries.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

FPGAs for SDR

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Figure 25

FPGAs Bridge the SDR Application Space

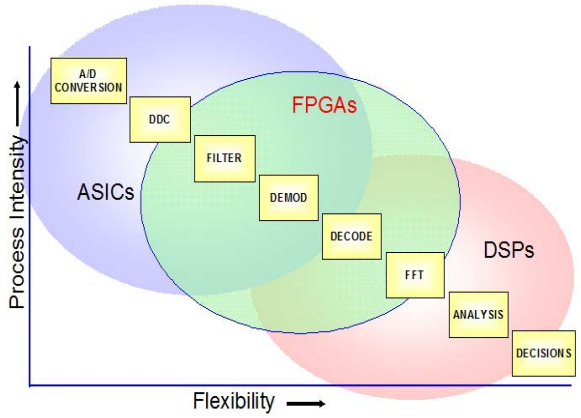


Figure 26

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 3500 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process-intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

Typical Pentek Products with Factory-Installed SDR IP Cores

Model	Input Channels	Sampling Freq (max)	Input Bits	DDC Chan.	Decimation Range	Output Bits	DUC Chan.	Interpol. Range	Chan. Out	Out Bits	Beam-former
71621	3	200 MHz	16	3	2–64K	16 or 24	1	2–512K	2	16	Yes
71624	2	200 MHz	16	34	512–8192	16	34	512–8192	2	–	No
71641	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	None	–	No
71741	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	None	–	No
71651	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	2	16	Yes
71751	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	2	16	Yes
71661	4	200 MHz	16	4	2–64K	16 or 24	None	None	None	–	Yes
71662	4	200 MHz	16	32	16–8K	24	None	None	None	–	No
71663	4	200 MHz	16	1100	–	–	None	None	None	–	No
71671	None	None	–	None	–	–	4	2–1024K	4	16	No
71771	None	None	–	None	–	–	4	2–1024K	4	16	No

Figure 27

The above chart shows the salient characteristics for some of Pentek's SDR products with factory-installed IP cores. All these products are available off-the-self and are in the Pentek datasheets and catalogs.

The chart provides information regarding the number of input channels, maximum sampling frequency of their A/Ds, and the number of bits. This information is followed by DDC characteristics such as number of DDC channels and the decimation range.

Other information that's specific to each core is included as well as an indication of the models that include a DUC, an interpolation filter and output D/A. As shown in the chart, many of these models include features that are critical for beamforming and direction-finding applications.

All the models shown here are XMC modules. As with all Pentek SDR products, these models are also available in PCI Express, OpenVPX, AMC, and CompactPCI formats as well.

For more information on these products, click on the Peoduct Selector below:

Click Here for the PRODUCT SELECTOR

Pentek, Inc. • One Park Way, Upper Saddle River, NJ 07458 • Tel: (201) 818-5900 • Fax: (201) 818-5904 • Email: info@pentek.com • http://www.pentek.com

FPGA Resource Comparison

	Virtex-II Pro VP	Virtex-4 FX, LX, SX	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX
Logic Cells	53K–74K	55K–110K	52K–155K	128K–314K	326K–693K
Slices*	23K–33K	24K–49K	8K–24K	20K–49K	51K–108K
CLB Flip-Flops	46K–66K	48K–98K	32K–96K	160K–392K	408K–864K
Block RAM (kb)	4,176–5,904	4,176–6,768	4,752–8,784	9,504–25,344	27,000–52,920
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E	DSP48E
DSP Slices	232–328	96–512	128–640	480–1,344	1,120–3,600
Serial Gbit Transceivers	N/A	0–20	12–16	20–24	28–80
PCI Express Support	N/A	N/A	N/A	Gen 2 x8	Gen 2 x8, Gen 3 x8
User I/O	852–996	576–960	480–680	600–720	700–1,000

*Virtex-II Pro and Virtex-4 Slices actually represent 2.25 Logic Cells;
*Virtex-5, Virtex-6 and Virtex-7 Slices actually represent 6.4 Logic Cells

Figure 28

The above chart compares the available resources in the five Xilinx FPGA families that are used or have been used in most of Pentek products.

- Virtex-II Pro: VP
- Virtex-4: FX, LX and SX
- Virtex-5: LX and SX
- Virtex-6: LX and SX
- Virtex-7: VX

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethenet ports.

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 500 MHz in V-4, to 550 MHz in V-5, to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.

Products

PMC, XMC, PCI Express, OpenVPX, AMC, FMC, and CompactPCI Software Radio and Supporting Products

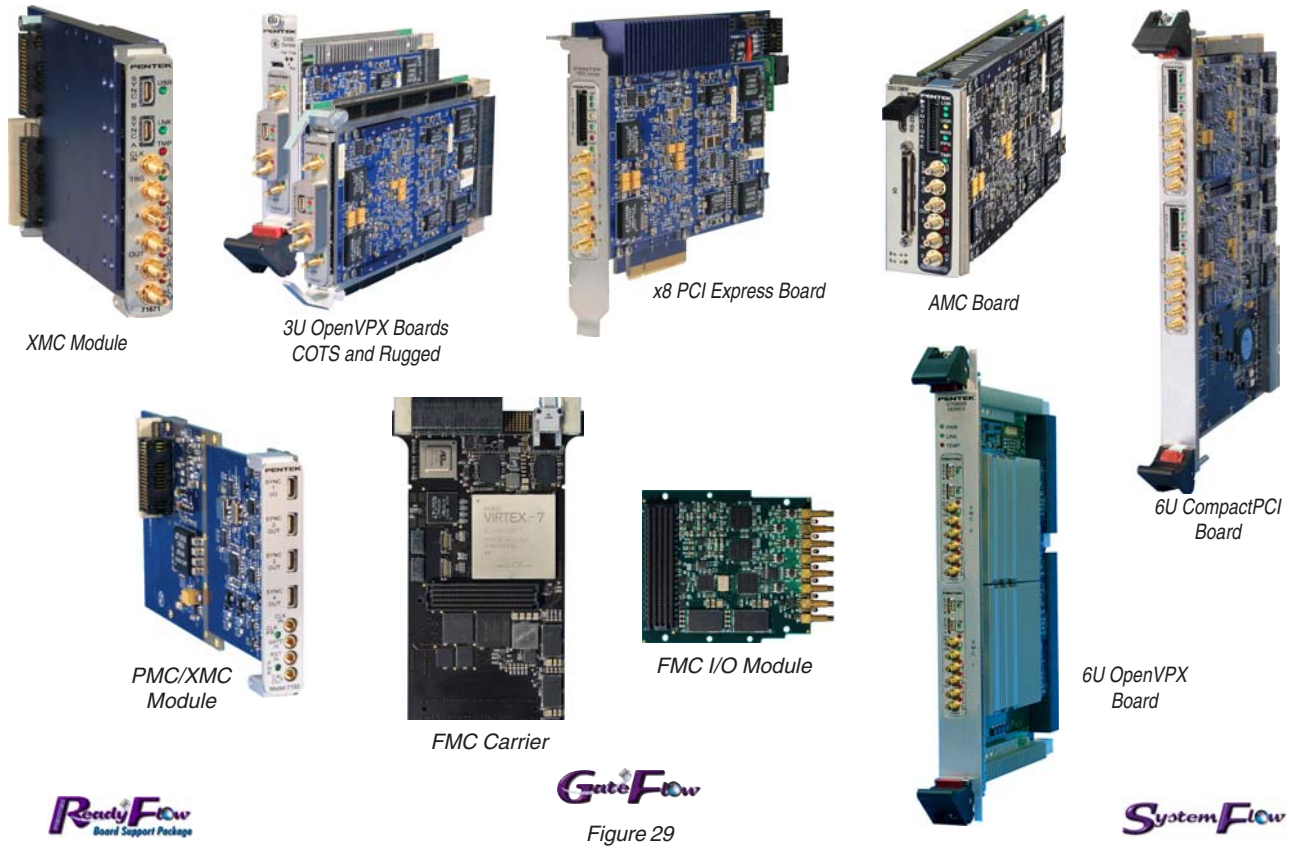


Figure 29

The Pentek family of board-level software radio products is the most comprehensive in the industry. All of these products are available in several formats to satisfy a wide range of requirements: PMC/XMC, PCI Express, 3U and 6U OpenVPX, AMC, FMC, 3U and 6U CompactPCI.

Software radio products are supported by clock synthesizer, synchronizer and distribution boards. These products are also available in the same formats as the software radio products.

In addition to their commercial versions, many of the above products are available in ruggedized versions up to and including conduction-cooled.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow® Board Support Package, the GateFlow® FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek high-speed recording systems are supported with SystemFlow® recording software that features a Windows®-based graphical user interface.

In addition to the product overviews presented in the pages that follow, active links to their datasheets on Pentek's website are included with each product.

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 71620 XMC • Model 78620 PCIe • Models 52620, 53620 3U VPX • Models 57620, 58620 6U VPX Model 56620 AMC • Model 72620 6U cPCI • Model 73620 3U cPCI • Model 74620 6U cPCI

Model 71620 XMC

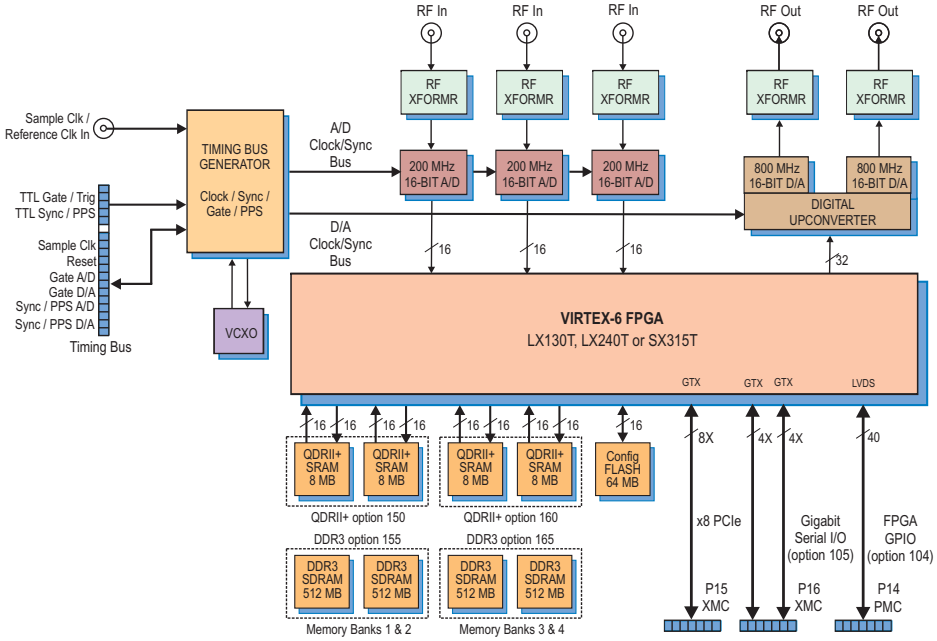


Figure 30

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or combinations.

Versions of the 71620 are also available as an x8 PCIe half-length board (Model 78620), 3U VPX (Models 52620 and 53620), 6U VPX (Models 57620 and 58620 dual density), AMC (Model 56620), 6U cPCI (Models 72620 and 74620 dual density), and 3U cPCI (Model 73620).

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 71720 XMC • Model 78720 PCIe • Models 52720, 53720 3U VPX • Models 57720, 58720 6U VPX Model 56720 AMC • Model 72720 6U cPCI • Model 73720 3U cPCI • Model 74720 6U cPCI

Model 71720 XMC

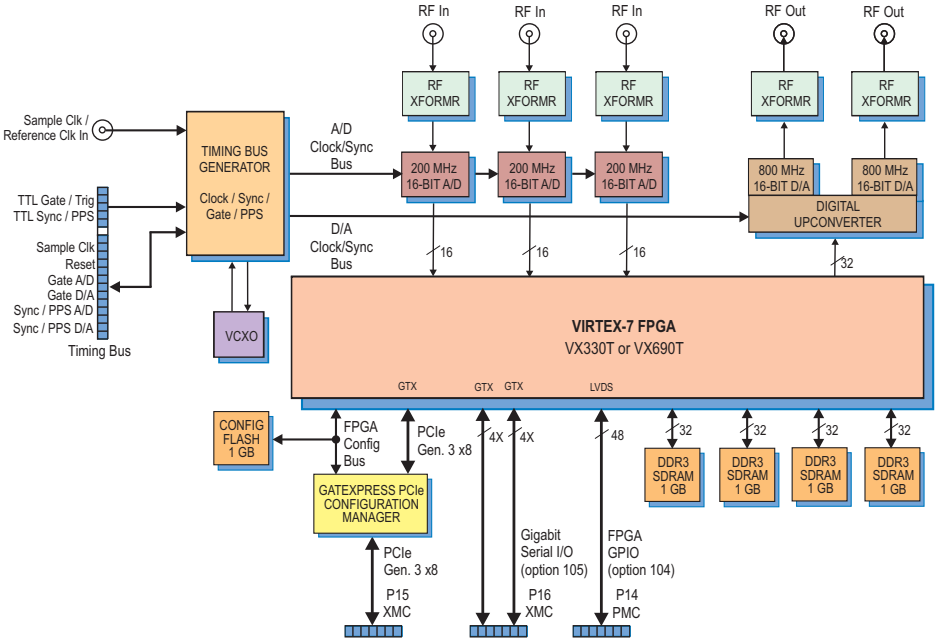


Figure 31

Model 71720 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

Multiple 71720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync.

Versions of the 71720 are also available as an x8 PCIe half-length board (Model 78720), 3U VPX (Models 52720 and 53720), 6U VPX (Models 57720 and 58720 dual density), AMC (Model 56720), 6U cPCI (Models 72720 and 74720 dual density), and 3U cPCI (Model 73620). GateXpress® is a sophisticated configuration manager for loading and reloading the Virtex-7 FPGA. More information is available in the next page.

GateXpress for FPGA-PCIe Configuration Management

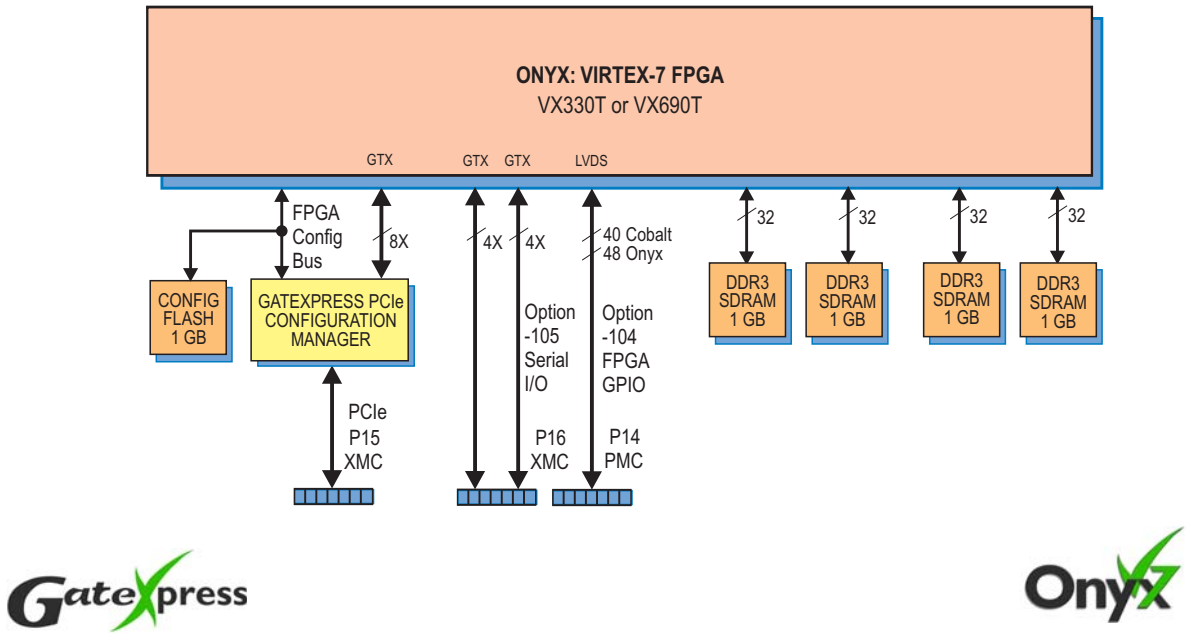


Figure 32

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-6 FPGA

Model 71621 XMC • Model 78621 PCIe • Models 52621, 53621 3U VPX • Models 57621, 58621 6U VPX Model 56621 AMC • Model 72621 6U cPCI • Model 73621 3U cPCI • Model 74621 6U cPCI

Model 71621 XMC

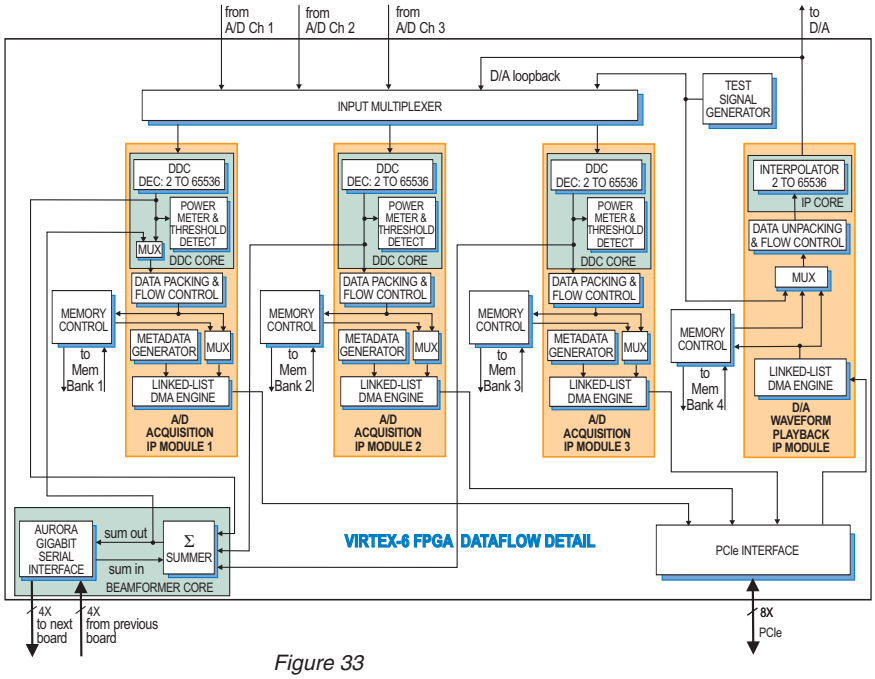


Figure 33

Model 71621 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71620 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71621 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71621 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 71621 are also available as an x8 PCIe half-length board (Model 78621), 3U VPX (Models 52621 and 53621), 6U VPX (Models 57621 and 58621 dual density), AMC (Model 56621), 6U cPCI (Models 72621 and 74621 dual density), and 3U cPCI (Model 73621).

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-7 FPGA

Model 56721 AMC • Model 71721 XMC • Model 78721 PCIe • Models 52721, 53721 3U VPX
Models 57721, 58721 6U VPX • Model 72721 6U cPCI • Model 73721 3U cPCI • Model 74721 6U cPCI

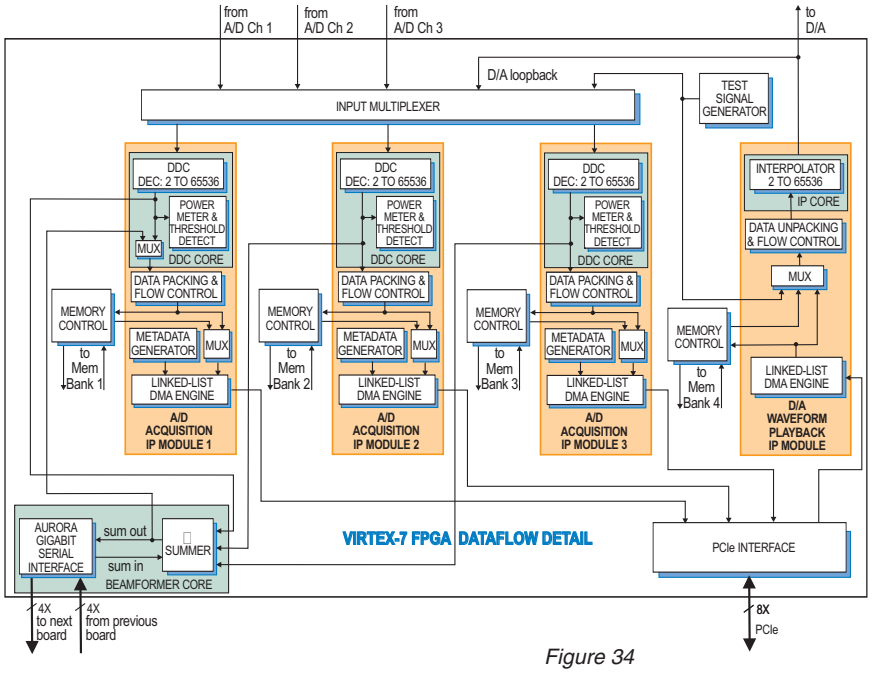


Figure 34

Model 56721 AMC

Onyx

GateXpress See page 21

Model 56721 is a member of the Onyx family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter based on the Model 71720 described previously, it includes factory-installed IP cores to enhance the performance of the 71720 and address the requirements of many applications.

The 56721 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 56721 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 56721 are also available as an XMC module (Model 71721), x8 PCIe board (Model 78721), 3U VPX (Models 52721 and 53721), 6U VPX (Models 57721 and 58721 dual density), 6U cPCI (Models 72721 and 74721 dual density), and 3U cPCI (Model 73721).

Dual-Channel 34-Signal Adaptive IF Relay, Installed IP Cores, Virtex-6 FPGA

Models 52624, 53624 3U VPX • Model 71624 XMC • Model 78624 PCIe • Model 56624 AMC
Models 57624, 58624 6U VPX • Model 72724 6U cPCI • Model 73624 3U cPCI • Model 74624 6U cPCI

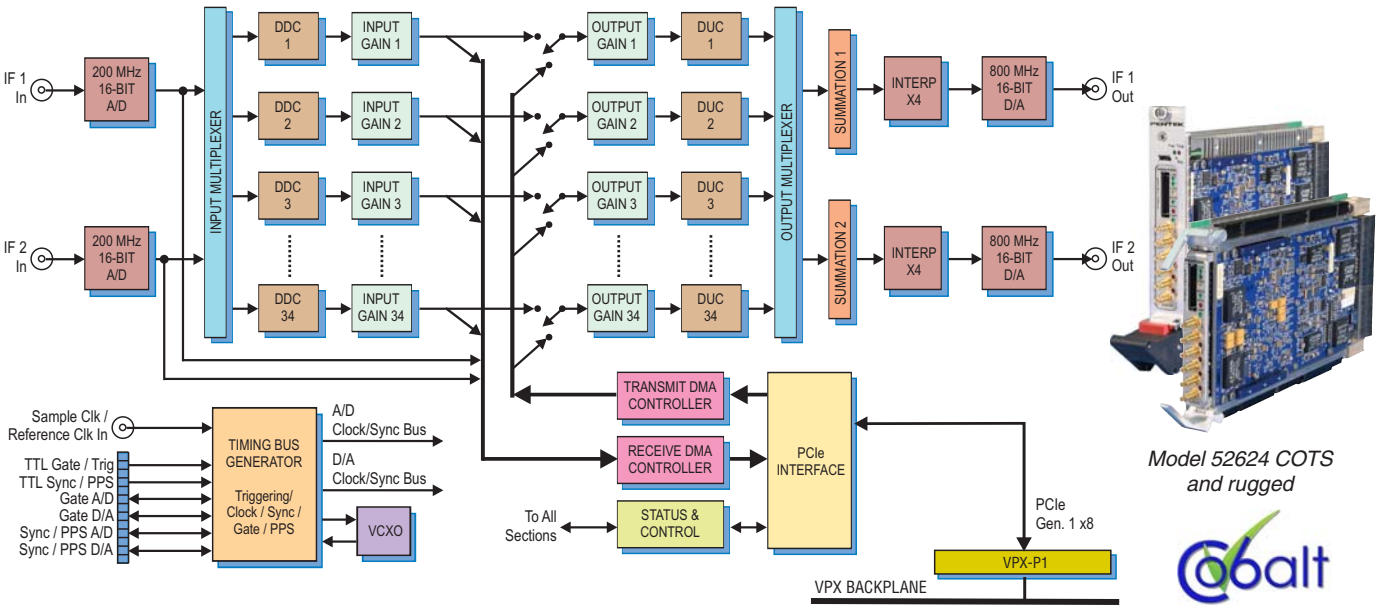


Figure 35

Model 52624 is a member of the Cobalt® family of high-performance 3U OpenVPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

The 52624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

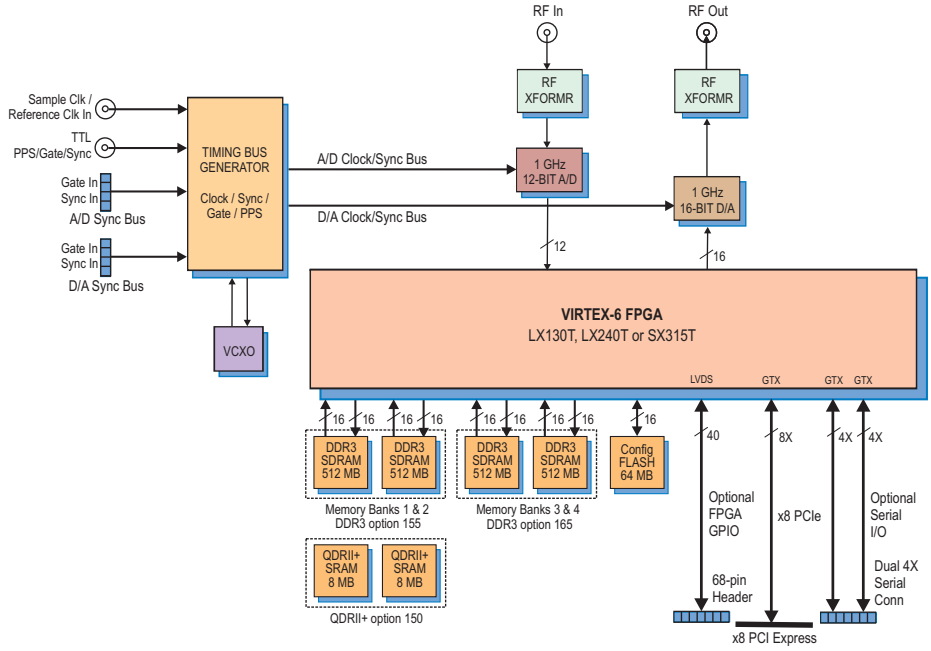
The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay. A PCIe Gen 1 system interface supports control, status and data transfers.

The Model 52624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Versions of the 52624 are also available as a different 3U VPX (Model 53624), 6U VPX (Models 57624 and 58624 with dual density), XMC module (Model 71624), an x8 PCIe board (Model 78624), AMC (Model 56624), 6U cPCI (Models 72624 and 74624 dual density), and 3U cPCI (Model 73624).

1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA

Model 78630 PCIe • Model 71630 XMC • Model 52630, 53630 3U VPX • Model 57630, 58630 6U VPX Model 56630 AMC • Model 72630 6U cPCI • Model 73630 3U cPCI • Model 74630 6U cPCI



Model 78630 x8 PCIe

Figure 36

Model 78630 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application- specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 78630's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations.

Versions of the 78630 are also available as an XMC module (Model 71630), 3U VPX (Models 52630 and 53630), 6U VPX (Models 57630 and 58630 with dual density), AMC (Model 56630), 6U cPCI (Models 72630 and 74630 with dual density), and 3U cPCI (Model 73630).

1 GHz A/D, 1 GHz D/A, Virtex-7 FPGA

Model 71730 XMC • Model 78730 PCIe • Model 52730, 53730 3U VPX • Model 57730, 58630 6U VPX Model 56730 AMC • Model 72730 6U cPCI • Model 73730 3U cPCI • Model 74730 6U cPCI

Model 71730 XMC

Onyx

GateXpress See page 21

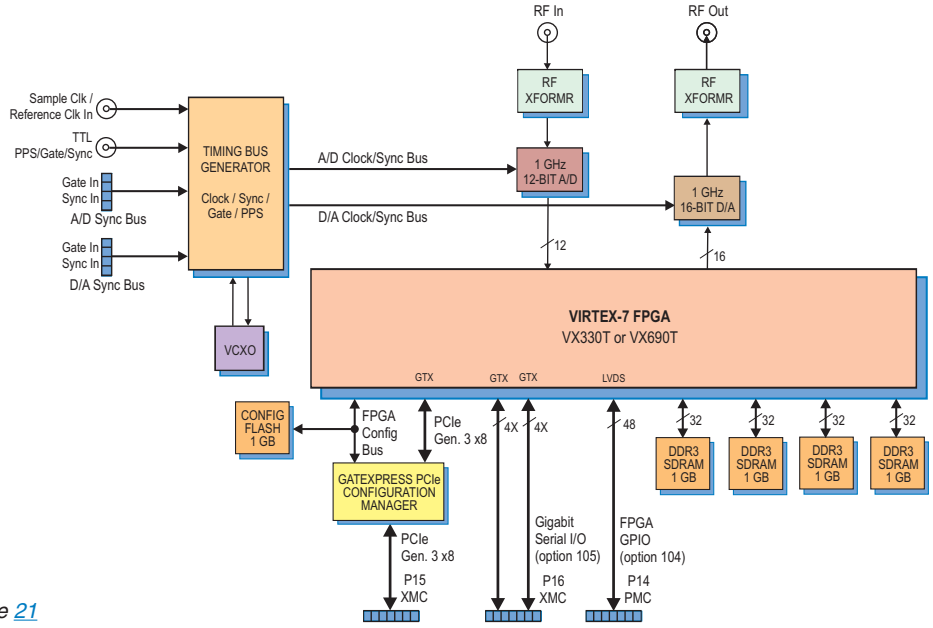


Figure 37

Model 71730 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71730 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

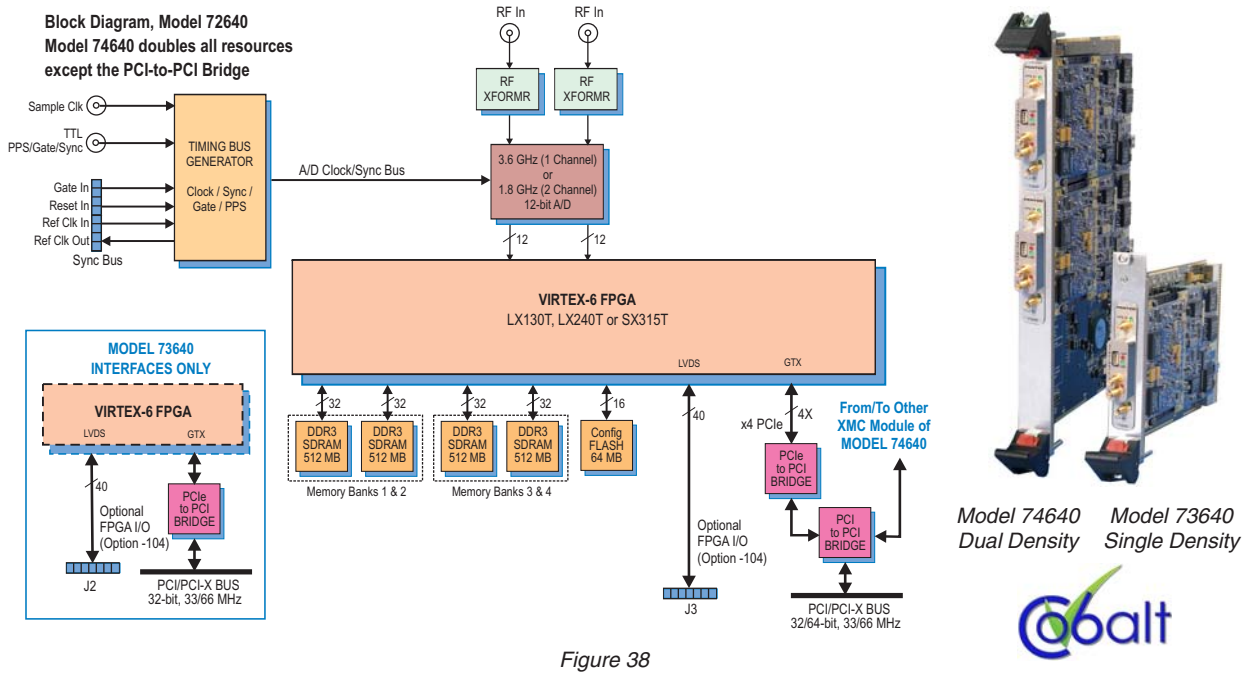
Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71730 to operate without the need to develop any FPGA IP.

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a TI ADS5400 1 GHz, 12-bit A/D converter. The digital outputs are delivered into the Virtex-7 FPGA for signal processing, etc.

Versions of the 71730 are also available as an x8 PCIe half-length board (Model 78730), 3U VPX (Models 52730 and 53730), 6U VPX (Models 57730 and 58730 dual density), AMC (Model 56730), 6U cPCI (Models 72730 and 74730 with dual density), and 3U cPCI (Model 73730).

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA

Model 72640 6U cPCI • Model 73640 3U cPCI • Model 74640 6U cPCI • Model 71640 XMC
Model 78640 PCIe • Models 52640, 53640 3U VPX • Models 57640, 58640 6U VPX • Model 56640 AMC



Model 74640 Dual Density *Model 73640 Single Density*

Figure 38

Models 72640, 73640 and 74640 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

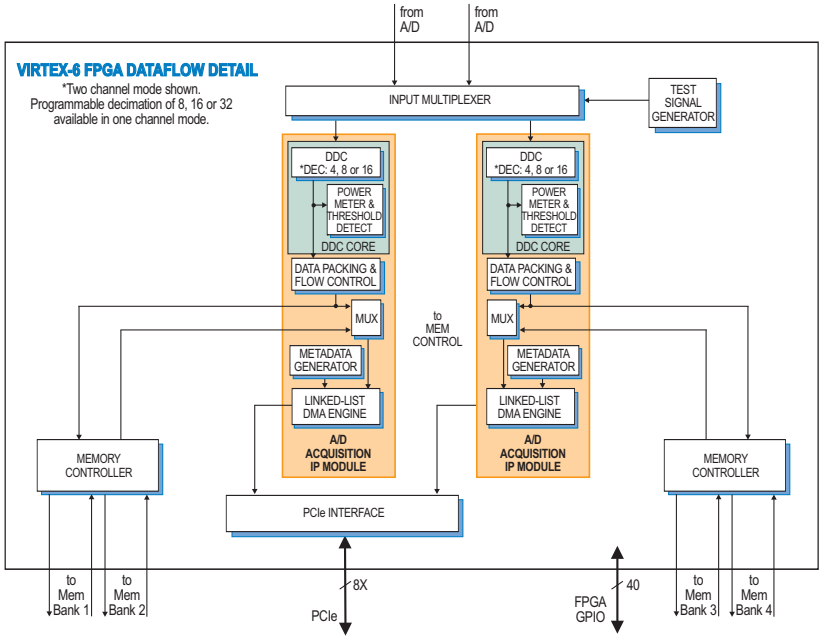
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing an input range of +2 to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 isa dual density 6U cPCI board; also available are an XMC (Model 71640), x8 PCIe (Model 78640), 3U VPX (Models 52640 and 53640), 6U VPX (Models 57640 and 58640 dual density), and AMC (Model 56640).

1- Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-6 FPGA

Model 56641 AMC • Model 71641 XMC • Model 78641 PCIe • Models 52641, 53641 3U VPX Models 57641, 58641 6U VPX • Model 72641 6U cPCI • Model 73641 3U cPCI • Model 74641 6U cPCI



Model 56641 AMC

Figure 39

Model 56641 is a member of the Cobalt family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. A very high-speed data converter based on the Model 56640 described in the previous page, it includes additional factory-installed IP cores to enhance the performance of the 56640 and address the requirements of many applications.

The 56641 factory-installed functions include an A/D acquisition IP module. In addition, within the FPGA is a powerful factory-installed DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Versions of the 56641 are also available as an XMC module (Model 71641), x8 PCIe board (Model 78641), 3U VPX (Models 52641 and 53641), 6U VPX (Models 57641 and 58641 dual density), 6U cPCI (Models 72641 and 74641 dual density), and 3U cPCI (Model 73641).

1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-7 FPGA

Model 71741 XMC • Model 78741 PCIe • Model 52741 3U VPX • Model 53741 3U VPX
Model 56741 AMC • Model 72741 6U cPCI • Model 73741 3U cPCI • Model 74741 6U cPCI

Model 71741 XMC

Onyx

GateXpress *See page 21*

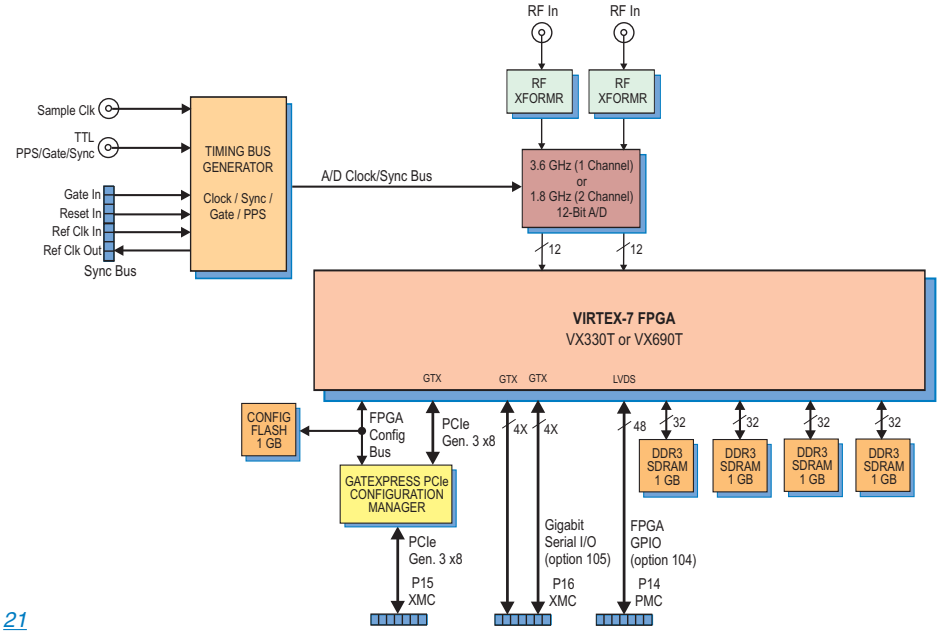


Figure 40

Model 71741 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

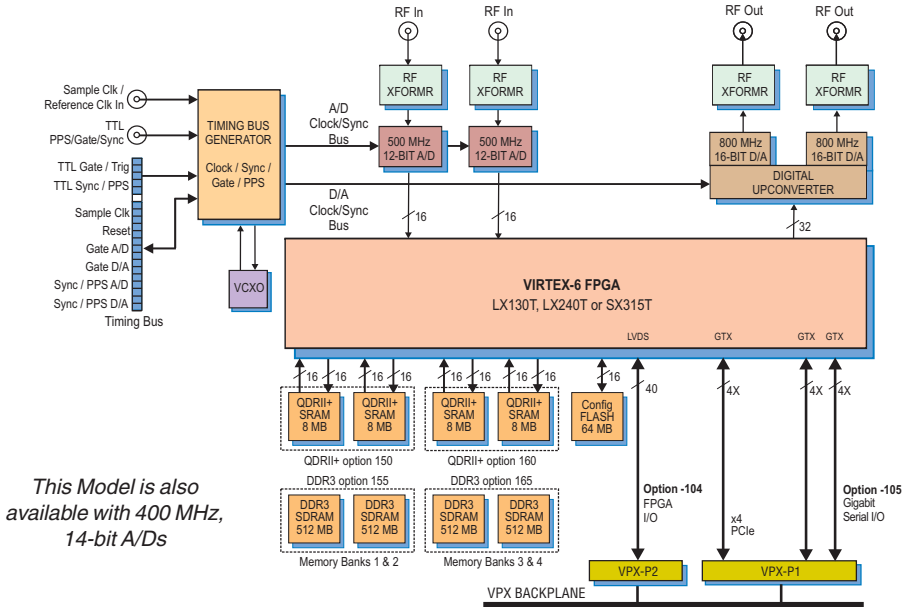
The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter.

The DDC core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation. In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s. In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x. See the dataflow diagram of the 71641 on the previous page for more detail.

Versions of the 71741 are also available as an x8 PCIe half-length board (Model 78741), 3U VPX (Models 52741 and 53741), 6U VPX (Models 57741 and 58741 (dual density), AMC (Model 56741), 6U cPCI (Models 72741 and 74741 with dual density), and 3U cPCI (Model 73741).

2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 52650, 53650 3U VPX • Models 57650, 58650 6U VPX • Model 71650 XMC • Model 78650 PCIe
Model 56650 AMC • Model 72650 6U cPCI • Model 73650 3U cPCI • Model 74650 6U cPCI



This Model is also available with 400 MHz, 14-bit A/Ds

Model 52650 3U VPX COTS and rugged

Figure 41

Model 52650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 52650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

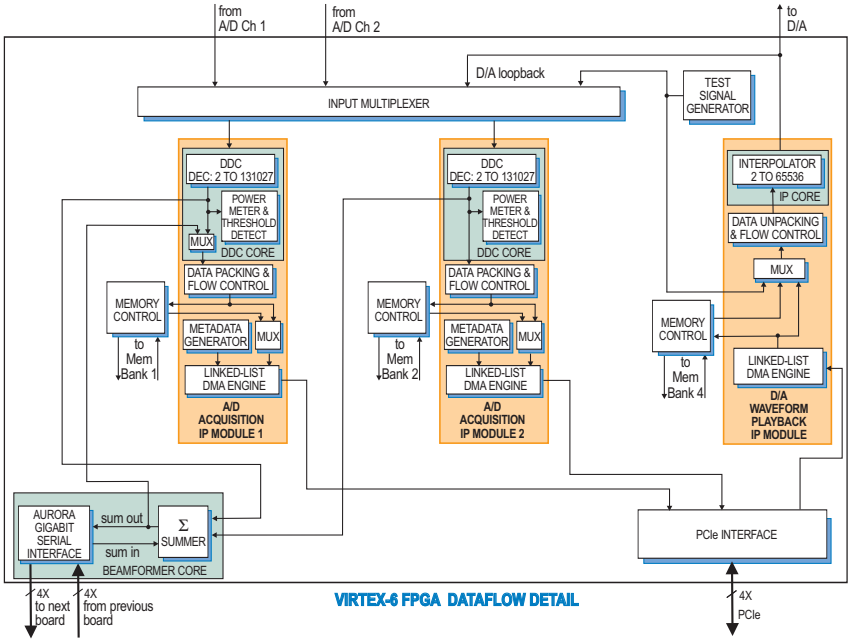
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations.

Versions of the 52650 are also available as a 3U VPX (Model 53650), 6U VPX (Models 57650 and 58650 dual density), XMC module (Model 71650), an x8 PCIe board (Model 78650), AMC (Model 56650), 6U cPCI (Models 72650 and 74650 dual density), and 3U cPCI (Model 73650).

2- or 4-Channel 500 MHz A/D, with DDCs, DUCs, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA

Model 72651 6U cPCI • Model 73651 3U cPCI • Model 74651 6U cPCI • Model 52651 3U VPX
Model 53651 3U VPX • Model 71651 XMC • Model 78651 PCIe • Model 56651 AMC



Model 74651 Dual Density *Model 73651 Single Density*

Figure 42

Models 72651, 73651 and 74651 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board. These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As and three or six banks of memory.

These models feature two or four A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP module in loopback mode.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

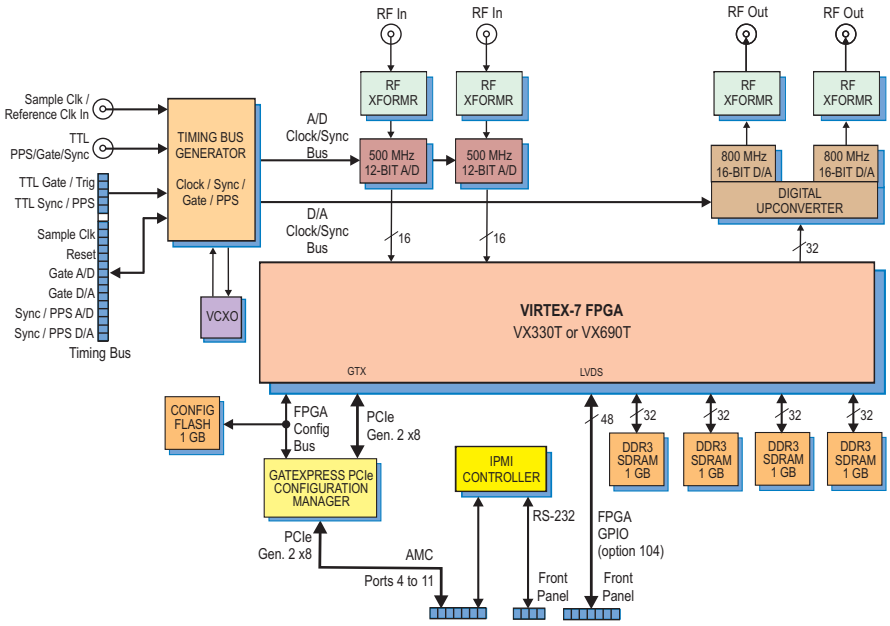
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output.

Model 72651 is a 6U cPCI board, while Model 73651 is a 3U cPCI board; Model 74651 a dual density 6U cPCI board; also available are an XMC (Model 71651), an x8 PCIe (Model 78651), 3U VPX (Models 52651 and 53651), 6U VPX (Models 57651 and 58651 dual density), and AMC (Model 56651).

2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 56751 AMC • Model 71751 XMC • Model 78751 PCIe • Models 52751, 53751 3U VPX
Model 57751, 58751 6U VPX • Model 72751 6U cPCI • Model 73751 3U cPCI • Model 74751 6U cPCI



Model 56751 AMC

See page 21

Figure 43

Model 56751 is a member of the Onyx family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56751 includes a general-purpose front-panel connector for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56751 to operate as a turnkey solution, See the block diagram on the previous page for more detail.

Versions of the 56751 are also available as an XMC module (Model 71751), x8 PCIe board (Model 78751), 3U VPX (Models 52751 and 53751), 6U VPX (Models 57751 and 58751 dual density), 6U cPCI (Models 72751 and 74751 dual density), and 3U cPCI (Model 73751).

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

Model 71660 XMC • Model 78660 PCIe • Models 52660, 53660 3U VPX • Models 57660, 58660 6U VPX Model 56660 AMC • Model 72660 6U cPCI • Model 73660 3U cPCI • Model 74660 6U cPCI

Model 71660 XMC

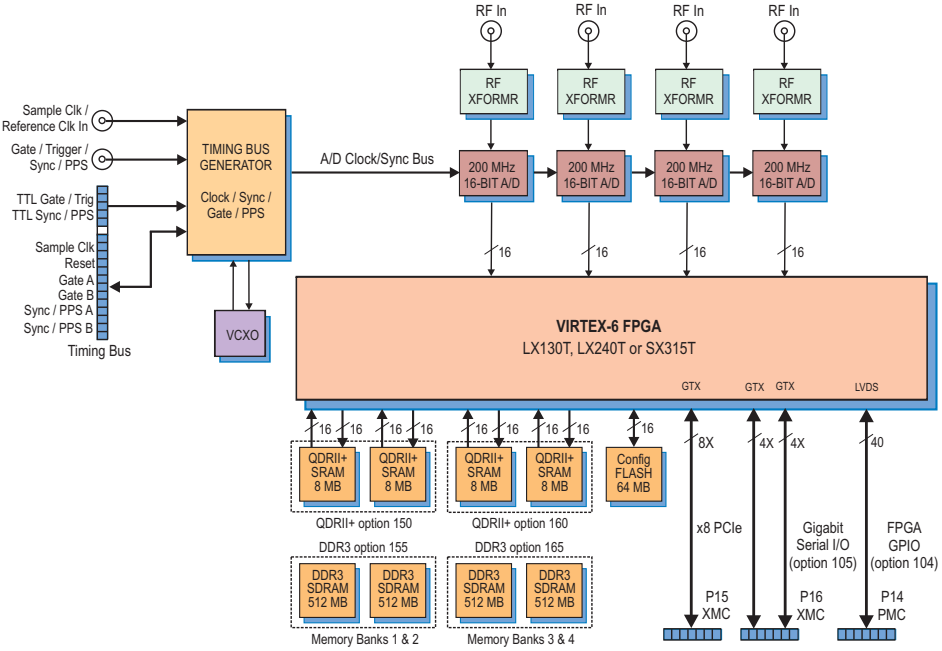


Figure 44

Model 71660 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71660 are also available as an x8 PCIe half-length board (Model 78660), 3U VPX (Models 52660 and 53660), 6U VPX (Models 57660 and 58660 dual density), AMC (Model 56660), 6U cPCI (Models 72660 and 74660 with dual density), and 3U cPCI (Model 73660).

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA

Model 71760 XMC • Model 78760 PCIe • Models 52760, 53760 3U VPX • Models 57760, 58760 6U VPX Model 56760 AMC • Model 72760 6U cPCI • Model 73760 3U cPCI • Model 74760 6U cPCI

Model 71760
XMC

Onyx

GateXpress See page 21

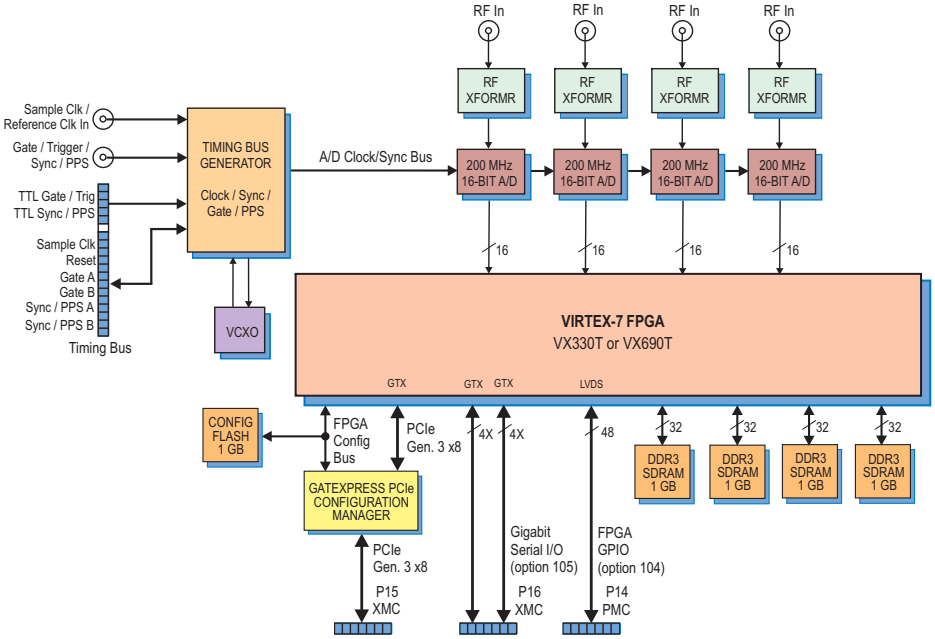


Figure 45

Model 71760 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data tranfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 71760 are also available as an x8 PCIe half-length board (Model 78760), 3U VPX (Models 52760 and 53760), 6U VPX (Models 57760 and 58760 (dual density), AMC (Model 56760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 71661 XMC • Model 78661 PCIe • Models 52661, 53661 3U VPX • Models 57661, 58661 6U VPX Model 56661 AMC • Model 72661 6U cPCI • Model 73661 3U cPCI • Model 74661 6U cPCI

Model 71661 XMC

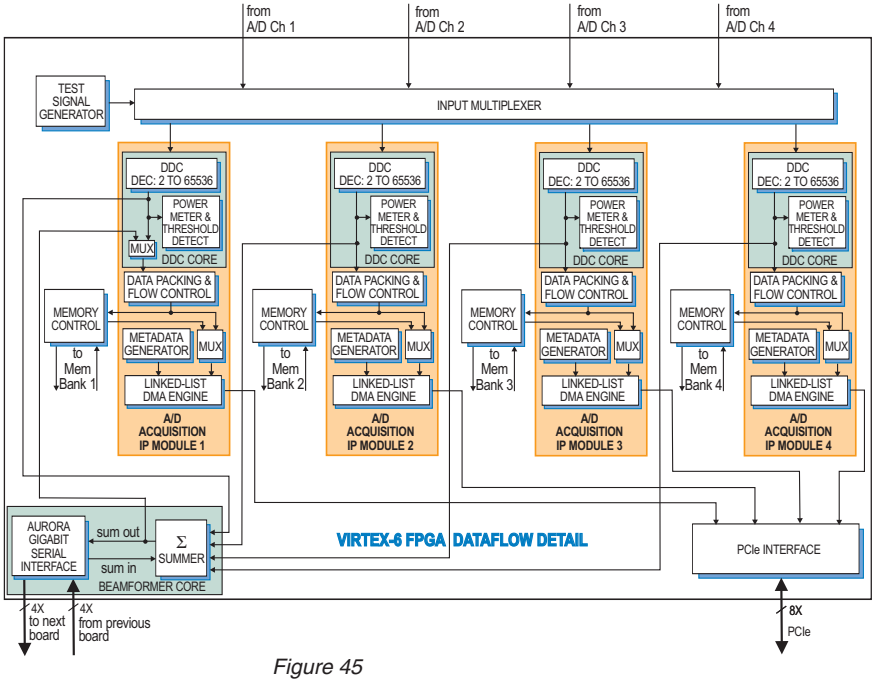


Figure 45

Model 71661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

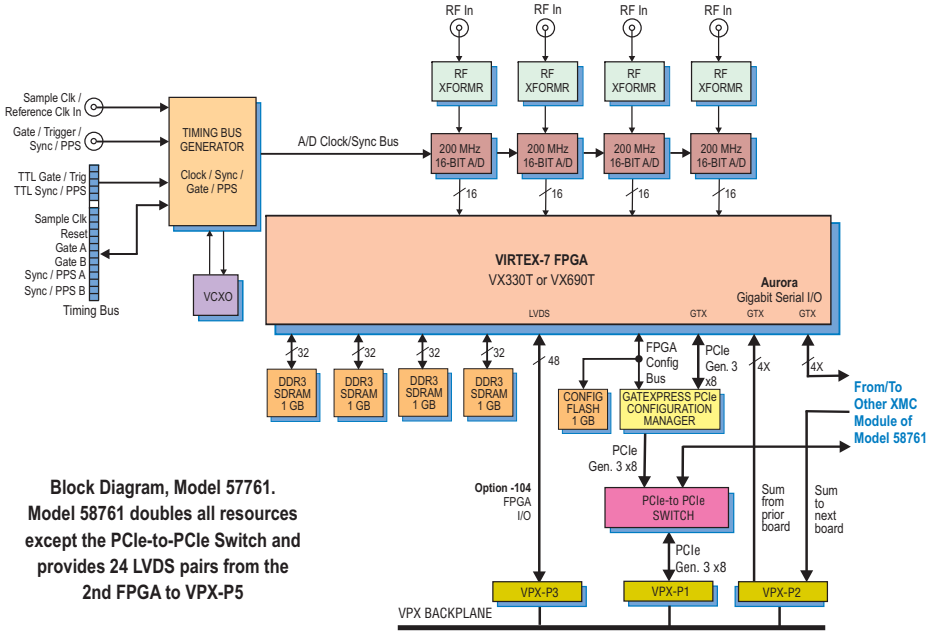
The 71661 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the 71661 are also available as an x8 PCIe half-length board (Model 78661), 3U VPX (Models 52661 and 53661), 6U VPX (Models 57661 and 58661 dual density), AMC (Model 56661), 6U cPCI (Models 72661 and 74661 with dual density), and 3U cPCI (Model 73661).

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-7 FPGA

Models 58761, 57761 6U VPX • Models 53761, 52761 3U VPX • Model 71761 XMC • Model 78761 PCIe
Model 56761 AMC • Model 72761 6U cPCI • Model 73761 3U cPCI • Model 74761 6U cPCI



Block Diagram, Model 57761. Model 58761 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

Model 58761 6U VPX Dual Density

See page 21

Figure 47

Model 58761 is a member of the Onyx family of high-performance OpenVPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter based on the Model 71760 described previously, it includes factory-installed IP cores to enhance the performance of the 71760 and address the requirements of many applications.

The 58761 factory-installed functions include eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, test signal generators, Aurora gigabit serial interfaces, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 58761 also features two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 58761's can be chained together via the built-in Xilinx Aurora gigabit serial interfaces.

Versions of the 58761 are also available as XMC (Model 71761), x8 PCIe half-length board (Model 78761), 3U VPX (Models 52761 and 53761), 6U VPX (Model 57761 single density), AMC (Model 56761), 6U cPCI (Models 72761 and 74761 dual density), and 3U cPCI (Model 73761).

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4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 78662 PCIe • Model 71662 XMC • Model 52662, 53662 3U VPX • Model 57662, 58662 6U VPX Model 56662 AMC • Model 72662 6U cPCI • Model 73662 3U cPCI • Model 74662 6U cPCI

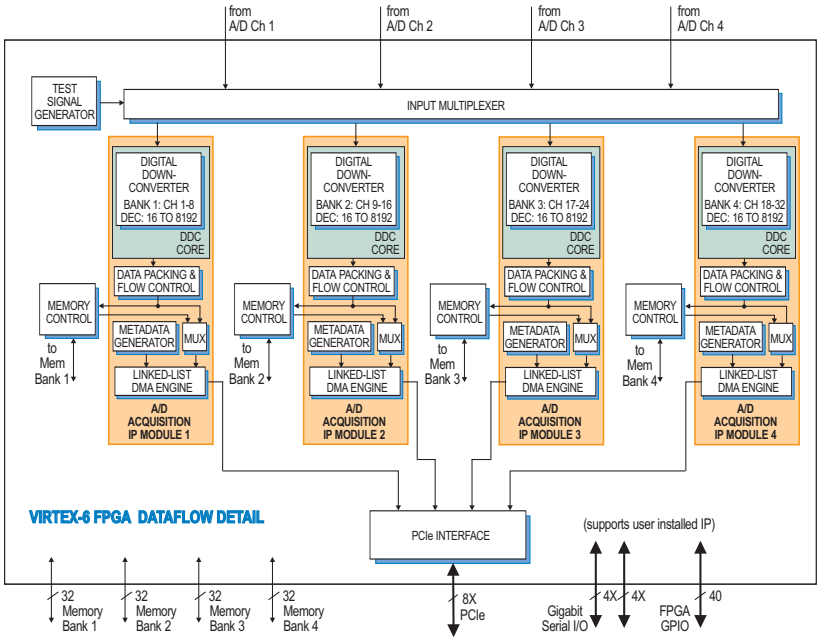


Figure 48

Model 78662
x8 PCIe

Model 78662 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 78662 are also available as an XMC module (Model 71662), 3U VPX (Models 52662 and 53662), 6U VPX (Models 57662 and 58662 with dual density), AMC (Model 56662), 6U cPCI (Models 72662 and 74662 with dual density), and 3U cPCI (Model 73662).

1100-Channel GSM Channelizer with Quad A/D, Virtex-6 FPGA

Models 53663, 52663 3U VPX • Model 71663 XMC • Model 78663 PCIe • Models 57663, 58663 6U VPX
Model 56663 AMC • Model 72663 6U cPCI • Model 73663 3U cPCI • Model 74663 6U cPCI

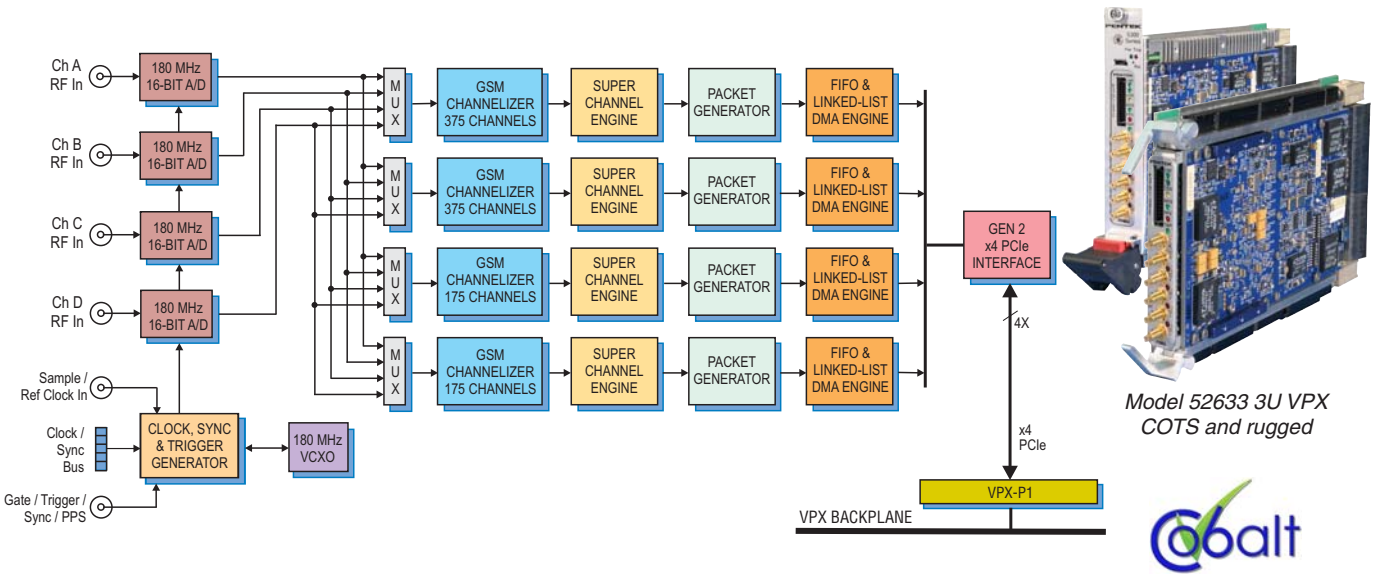


Figure 49

The Model 52663 accepts four analog inputs from an external analog RF tuner, such as the Pentek Model 8111, where the GSM RF bands are downconverted to an IF frequency. These IF signals are then digitized by four A/D converters and routed to four channelizer banks, which perform digital downconversion of all GSM channels to baseband. Two of the banks handle 175 channels for the lower GSM transmit/receive bands and two more banks handle 375 channels for the upper bands. The DDC channels within each bank are equally spaced at 200 kHz.

Each DDC output is resampled to a 4x symbol rate of 1.08333 MHz to simplify symbol recovery. Every four DDC outputs are combined into a frequency-division "super-channel" that allows transmission of all 1100 channels across the PCIe Gen. 2 x4 interface. The GSM channelizer IP core is supported with factory-installed FPGA functions including packet formation, time stamping, four DMA controllers, gating and triggering.

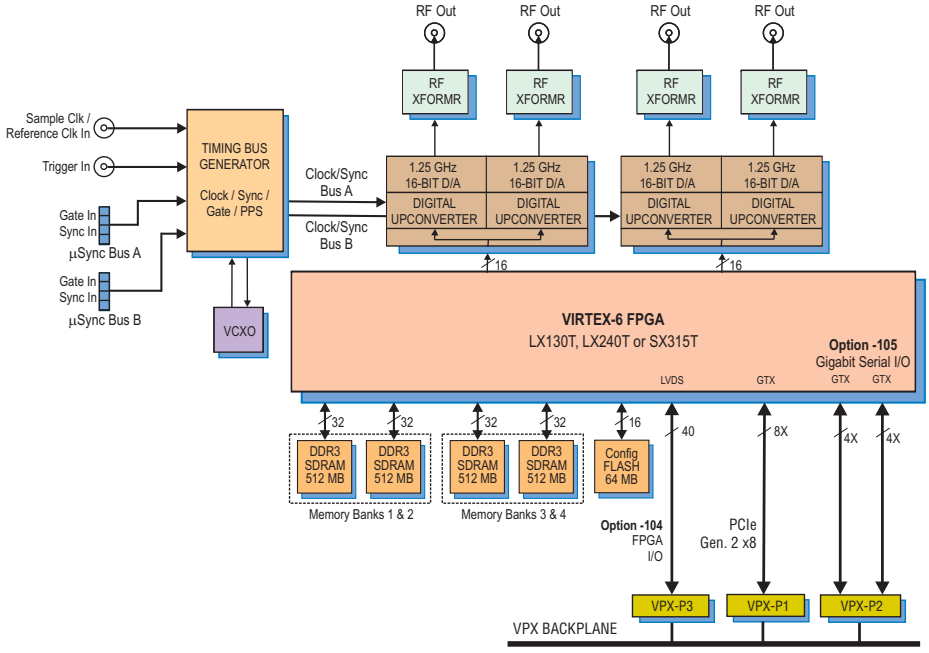
Super-channel packets are formed by appending enabled super-channel samples sequentially from each bank. Once complete, a unique super-channel packet header is inserted at the beginning of each packet for identification. The header contains a time stamp, a sequential packet count, the number of enabled super-channels, the DMA channel identifier, and other information.

The 52663 is ideal for mobile monitoring systems that must capture some or all of the 1100 uplink and downlink signals in both upper and lower GSM bands. This full-global system for mobile communications spectrum monitoring targets homeland security, government and military applications.

Versions of the 52633 are also available as an XMC module (Model 71663), an x8 PCIe half-length board (Model 78663), 3U VPX (Model 53663), 6U VPX (Models 57663 and 58663 with dual density), AMC (Model 56663), 6U cPCI (Models 72663 and 74663 with dual density), and 3U cPCI (Model 73663).

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA

Models 57670, 58670 6U VPX • Models 53670, 52670 3U VPX • Model 71670 XMC • Model 78670 PCIe
Model 56670 AMC • Model 72670 6U cPCI • Model 73670 3U cPCI • Model 74670 6U cPCI



Model 57670
6U VPX
Single Density

Figure 50

Model 57670 is a member of the Cobalt family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 57670 includes a front panel general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The Model 57670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 57670 to operate as a turnkey solution without the need to develop FPGA IP.

Versions of the 57670 are also available as XMC (Model 71670), x8 PCIe (Model 78670), 3U VPX (Models 52670 and 53670), 6U VPX (Model 58670 dual density), AMC (Model 56670), 6U cPCI (Models 72670 and 74670 dual density), and 3U cPCI (Model 73670).

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation, Virtex-6 FPGA

Model 71671 XMC • Model 78671 PCIe • Models 52671, 53671 3U VPX • Models 57671, 58671 6U VPX Model 56671 AMC • Model 72671 6U cPCI • Model 73671 3U cPCI • Model 74671 6U cPCI

Model 71671 XMC

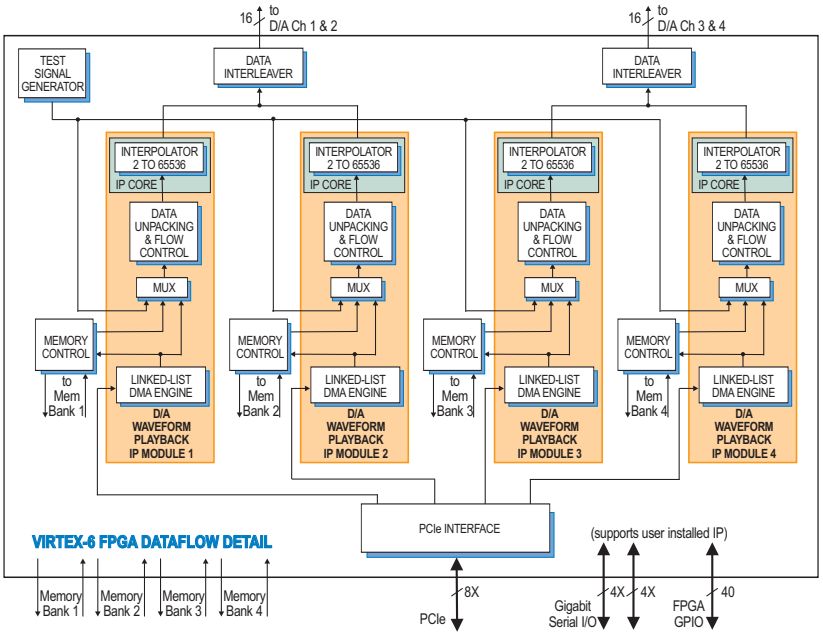


Figure 51

Model 71671 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71670 described previously, it includes factory-installed IP cores to enhance the performance of the 71670 and address the requirements of many applications.

The Model 56671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x.

In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems.

Versions of the 71671 are also available as an x8 PCIe half-length board (Model 78671), 3U VPX (Models 52671 and 53671), 6U VPX (Models 57671 and 58671 with dual density), AMC (Model 56671), 6U cPCI (Models 72671 and 74671 with dual density), and 3U cPCI (Model 73671).

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation, Virtex-7 FPGA

Model 71771 XMC • Model 78771 PCIe • Model 52771 3U VPX • Model 53771 3U VPX
Model 56771 AMC • Model 72771 6U cPCI • Model 73771 3U cPCI • Model 74771 6U cPCIl

Model 71771 XMC

Onyx

GateXpress

See page 21

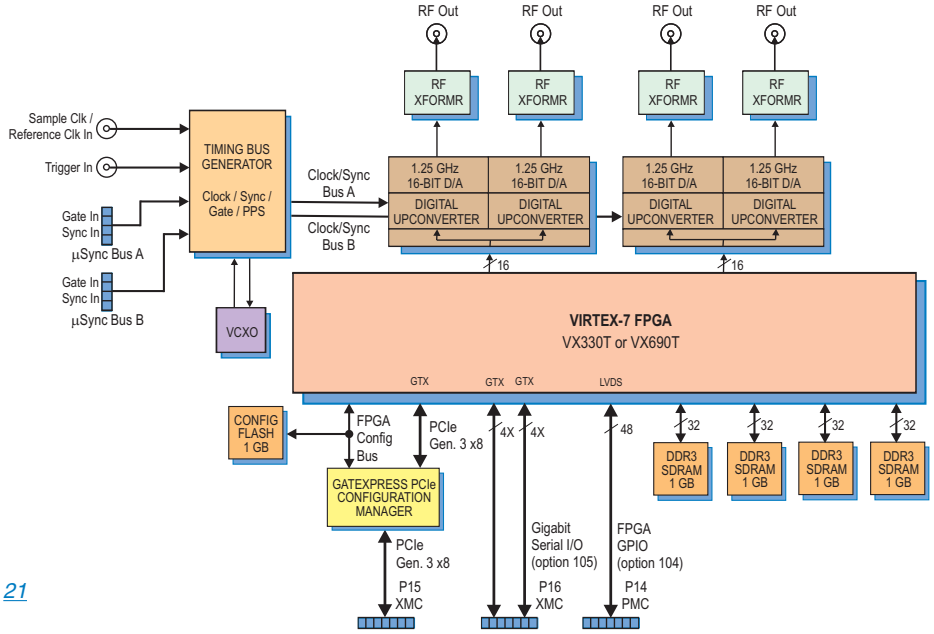


Figure 52

Model 71771 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four digital upconverters, four D/As with a wide range of programmable interpolation factors, and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71771 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

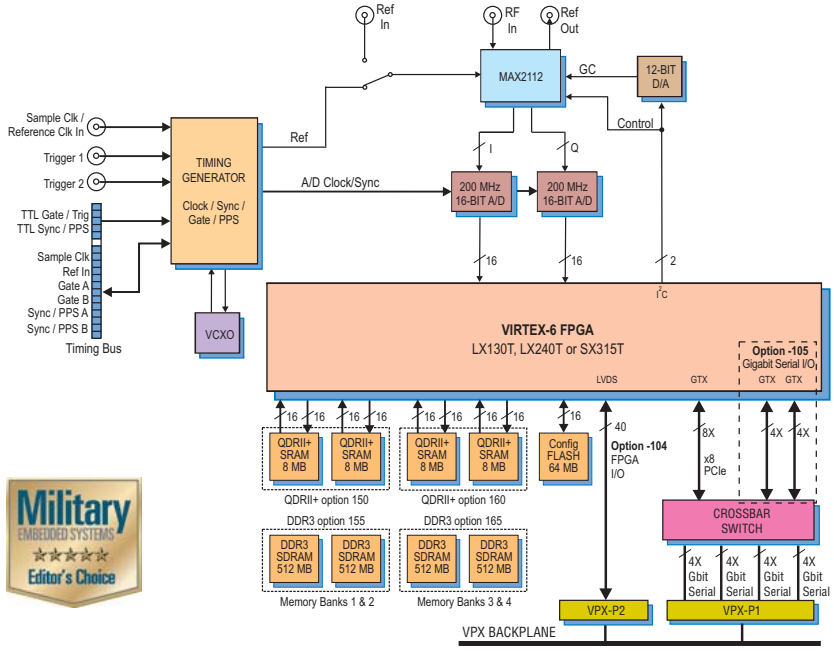
The Model 71771 factory-installed functions include a sophisticated D/A Waveform Playback IP module to support waveform generation to the four D/As from tables stored in on-board or off-board host memory.

Two Texas Instruments DAC3484s provide four DUC and D/A channels with interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71771 features an FPGA-based interpolation engine. The combined total interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. See the block diagram of the 71671 on the previous page for more detail.

Versions of the 71771 are also available as an x8 PCIe half-length board (Model 78771), 3U VPX (Models 52771 and 53771), 6U VPX (Models 57771 and 58771 with dual density), AMC (Model 56771), 6U cPCI (Models 72771 and 74771 with dual density), and 3U cPCI (Model 73771).

L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA

Models 53690, 52690 3U VPX • Model 71690 XMC • Model 78690 PCIe • Models 57690, 58690 6U VPX Model 56690 AMC • Model 72690 6U cPCI • Model 73690 3U cPCI • Model 74690 6U cPCI



Model 53690 3U VPX COTS and rugged

Figure 53

Model 53690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) down-converting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the 53690 are also available as an XMC (Model 71690), an x8 PCI board (Model 78690), 3U VPX (Model 52690), 6U VPX (Models 57690 and 58690 dual density), AMC (Model 56690), 6U cPCI (Models 72690 and 74690 dual density), and 3U cPCI (Model 73690).

Pentek, Inc. • One Park Way, Upper Saddle River, NJ 07458 • Tel: (201) 818-5900 • Fax: (201) 818-5904 • Email: info@pentek.com • http://www.pentek.com

3U OpenVPX Virtex-7 Processor and FMC Carrier

Model 5973 - FMC

Model 5973
FMC

See page 21

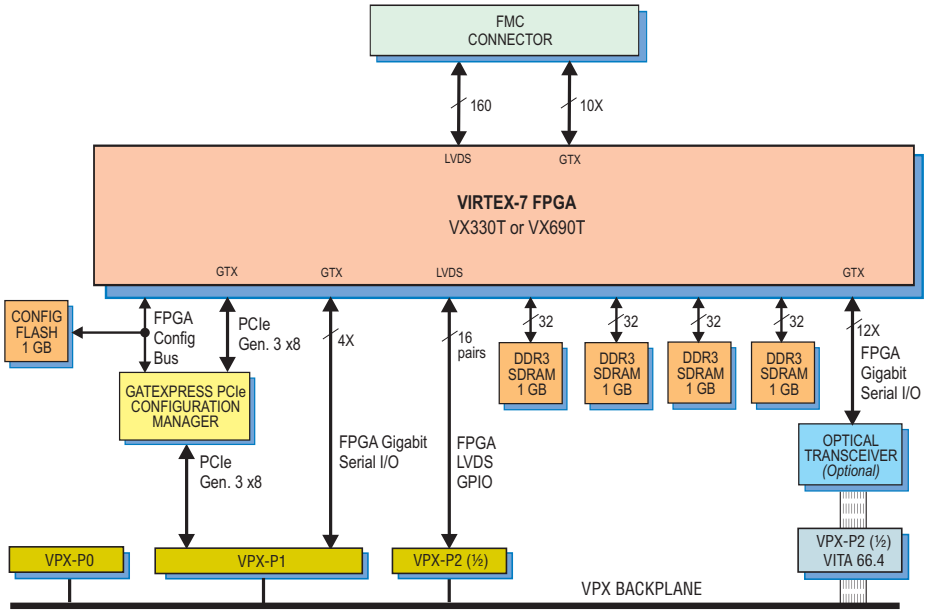


Figure 54

The Flexor® Model 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

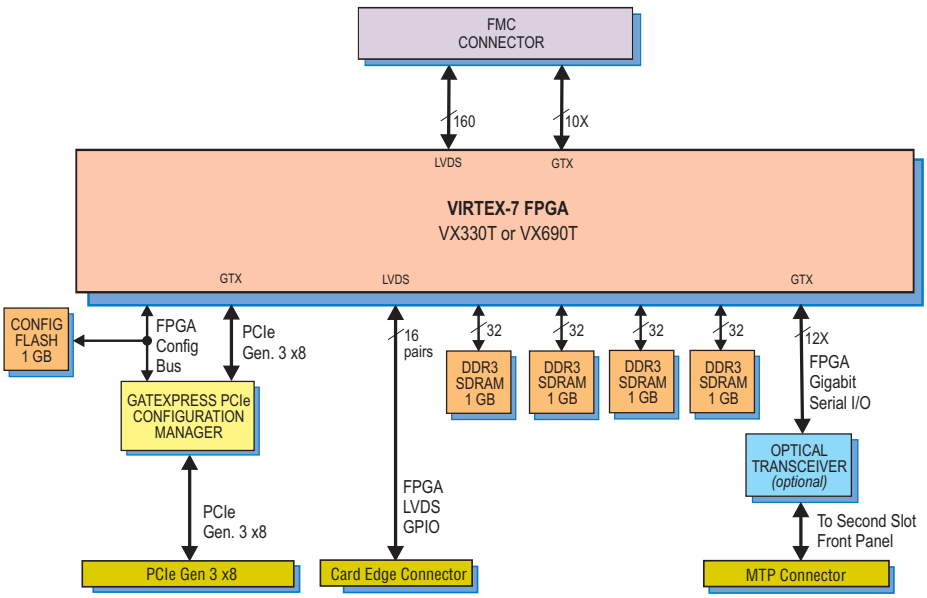
When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked- list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

Model 7070 - FMC



Model 7070 shown with Model 3312 multichannel A/D & D/A FMC module

FlexorGateXpress

See page 21

Figure 55

The Flexor Model 7070 is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample -count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070 and installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A

Model 3312 - FMC

Model 3312
FMC

Flexor

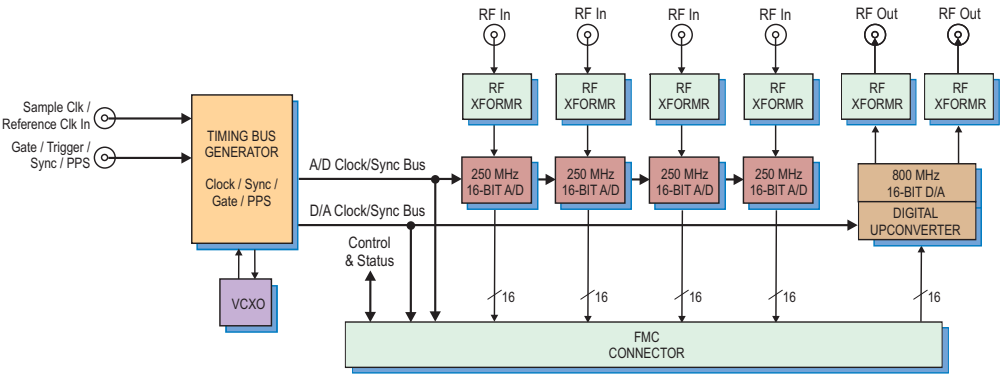


Figure 56

The Flexor Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe FMC Carrier, the board-set becomes a turnkey data acquisition and signal generation solution. For applications that require custom processing, the board set is an ideal IP development and deployment subsystem.

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

The Model 3312 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own FPGA IP for operating the FMC.

While users will find the Model 3312 an excellent analog interface to the VC707, or any compatible FMC carrier, the true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

When used with the 5973 or the 7070, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

8-Channel 250 MHz 16-bit A/D

Model 3316 - FMC

Model 3316
FMC

Flexor

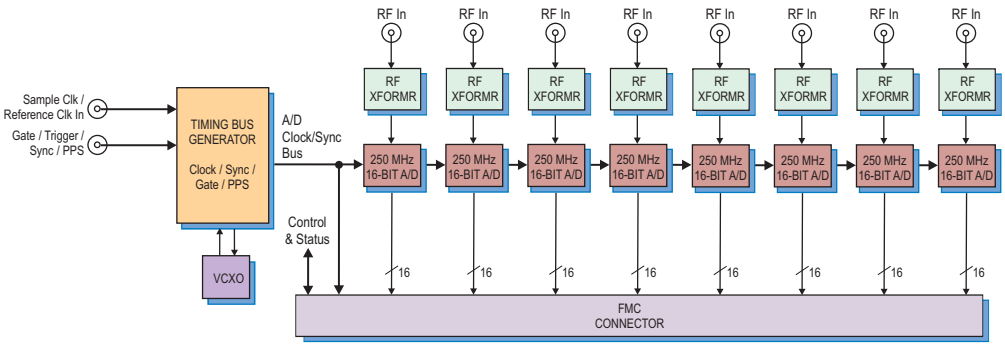


Figure 57

The Flexor Model 3316 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, on-board programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe FMC Carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

The Model 3316 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own FPGA IP for operating the FMC.

While users will find the Model 3316 an excellent analog interface to the VC707, or any compatible FMC carrier, the true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

When the 3316 is installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

8-Channel 250 MHz A/D with Digital Downconverters - 3U OpenVPX

FlexorSet Model 5973-317

Model 5973-317

GateFlow
ReadyFlow Board Support Package
Flexor
GateXpress See page 21

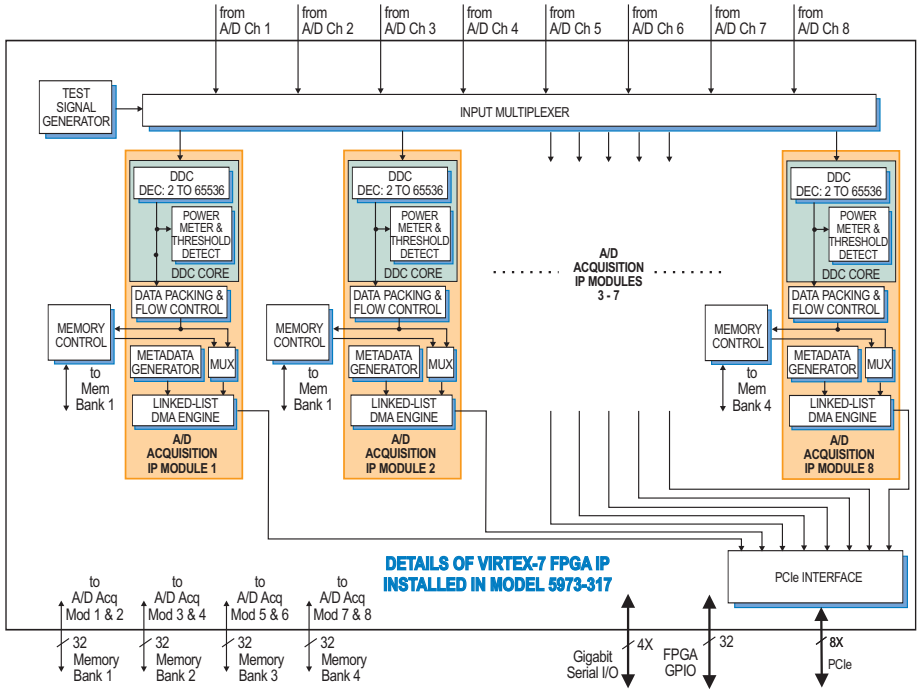


Figure 58

Model [5973-317](#) is a member of the Flexor family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 5973-317 includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board set, the [5973-317](#) includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

8-Channel 250 MHz A/D with Digital Downconverters - x8 PCIe

FlexorSet Model 7070-317

Model 7070-317

GateFlow
ReadyFlow Board Support Package
Flexor
GateXpress See page 21

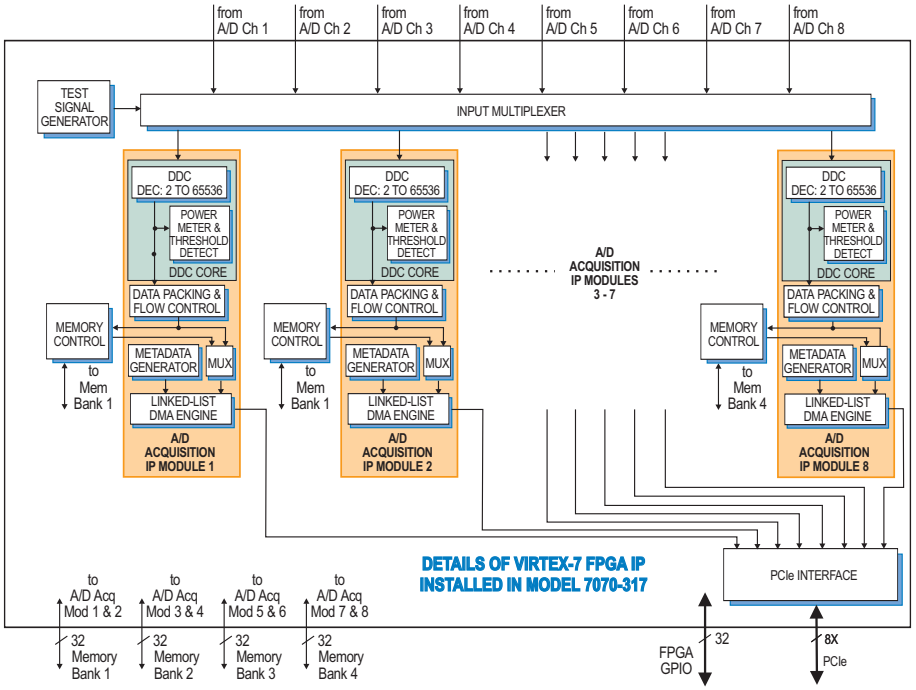


Figure 59

Model 7070-317 is a member of the Flexor family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-317 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

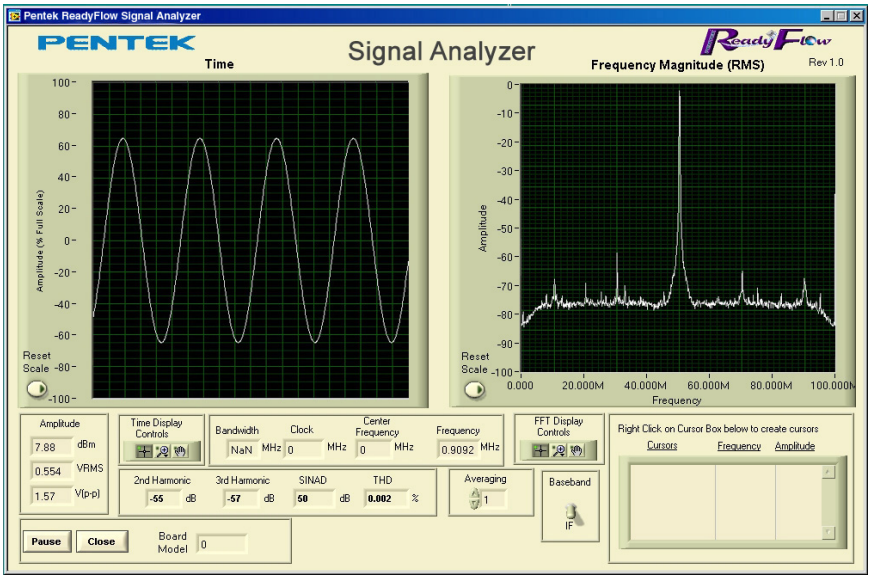
When delivered as an assembled board set, the 7070-317 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

PC Development System for PCIe Cobalt, Onyx and Flexor Boards

Model 8266



Model 8266

SPARK Development Systems

ReadyFlow Board Support Package

Figure 60

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

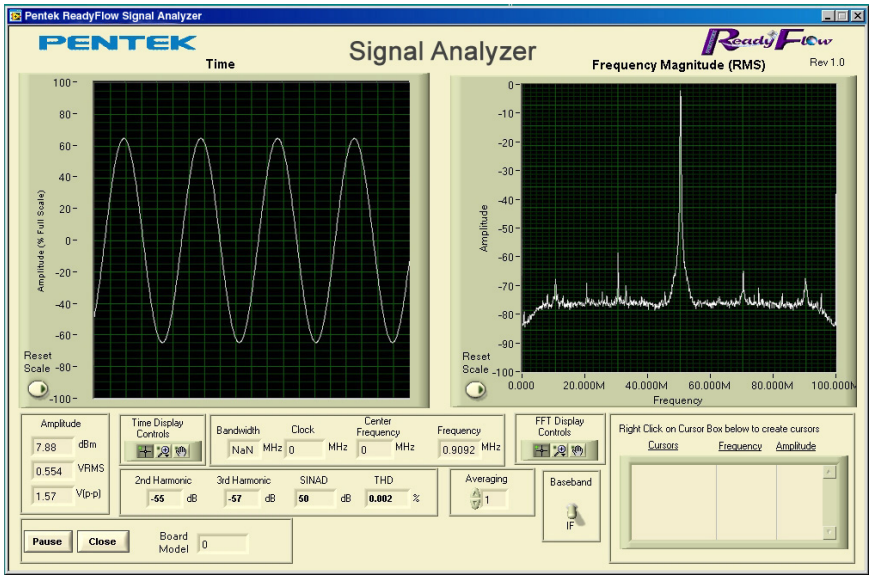
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek boards. A 1000-W power supply guarantees more than enough power for additional boards.

3U OpenVPX Development System for Cobalt, Onyx and Flexor Boards

Model 8267



Model 8267

SPARK Development Systems

ReadyFlow Board Support Package

Figure 61

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt, Onyx and Flexor software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

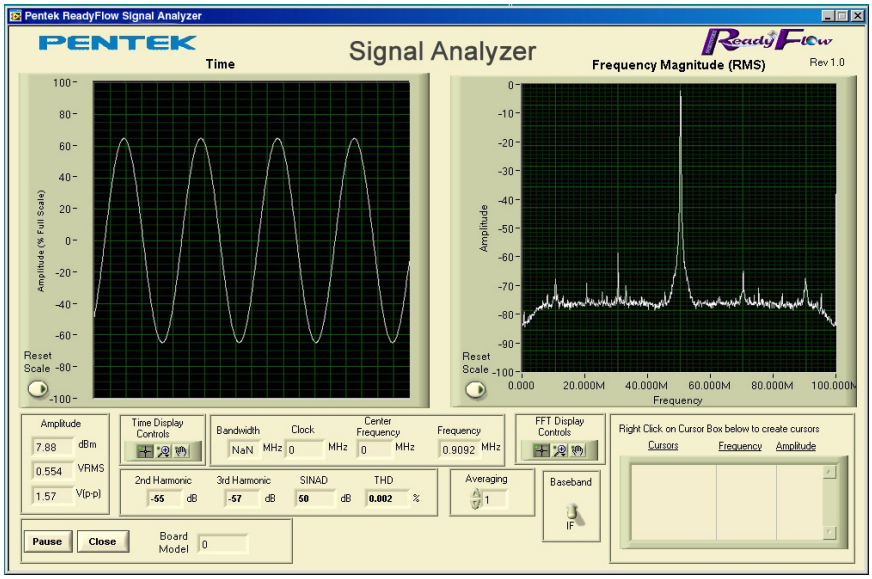
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

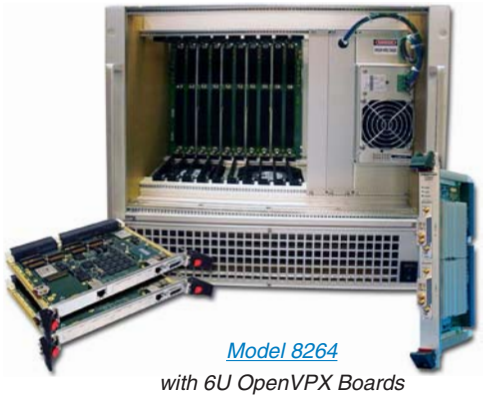
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies gurantee more than adequate power for all installed boards.

6U OpenVPX Development System for Cobalt and Onyx Boards

Model 8264





Model 8264
with 6U OpenVPX Boards

SPARK Development Systems

ReadyFlow Board Support Package

Figure 62

The Model 8264 is a fully-integrated, 6U VPX development system for Pentek Cobalt and Onyx software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

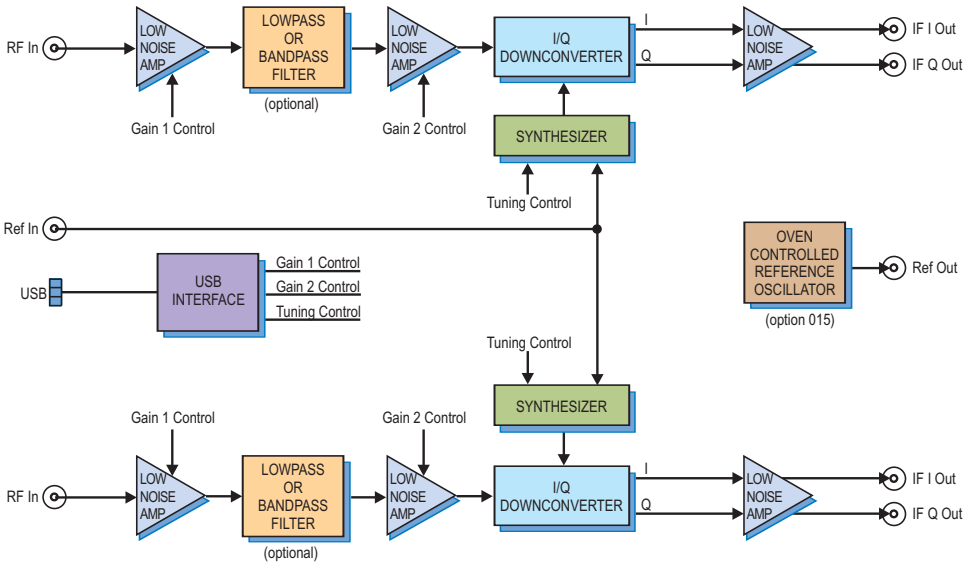
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

Built on a professional 6U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19" 6U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies gurantee more than adequate power for all installed boards.

Bandit Two-Channel Analog RF Wideband Downconverter

Model 7820 PCIe • Model 7120 XMC • Models 5220, 5320 3U VPX • Models 5720, 5820 6U VPX
Model 5620 AMC • Model 7220 6U cPCI • Model 7320 3U cPCI • Model 7420 6U cPCI



Model 7820 PCIe

Figure 63

The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband down-converter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and SIGINT.

The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input. An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression. The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

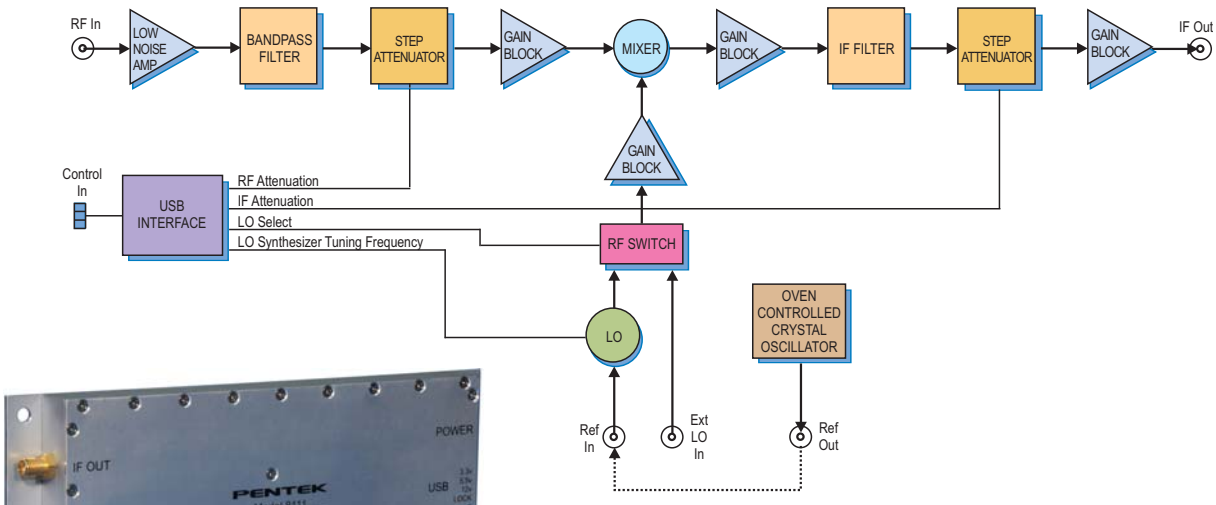
The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements.

Versions of the 7820 are also available as an XMC module (Model 7120), 3U VPX (Models 5220 and 5320), 6U VPX (Models 5720 and 5820 with dual density), AMC (Model 5620), 6U cPCI (Models 7220 and 7420 with dual density), and 3U cPCI (Model 7320).

Bandit Modular Analog RF Downconverter Series

Model 8111



Model 8111

Figure 64

The Bandit Model 8111 provides a series of high-performance, stand-alone RF slot receiver modules. Packaged in a small, shielded enclosure with connectors for easy integration into RF systems, the modules offer programmable gain, high dynamic range and a low noise figure. With input options to cover specific frequency bands of the RF spectrum, and an IF output optimized for A/D converters, the 8111 is an ideal solution for amplifying and down-converting antenna signals for communications, radar and signal intelligence systems.

The 8111 accepts RF signals on a front panel SMA connector. An LNA (Low Noise-figure Amplifier) is provided along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Seven different input-frequency band options are offered, each tunable across a 400 MHz band, with an overlap of 100 MHz between adjacent bands. As a group, these seven options accommodate RF input signals from 800 MHz to 3.000 GHz as follows:

Option	Frequency Band
001	800-1200 MHz
002	1100-1500 MHz
003	1400-1800 MHz
004	1700-2100 MHz
005	2000-2400 MHz
006	2300-2700 MHz
007	2600-3000 MHz

An 80 MHz wide IF output is provided at a 225 MHz center frequency . This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

Multifrequency Clock Synthesizer

Model 7190 PMC • Model 7890 PCIe • Model 5390 3U VPX • Models 5790, 5890 6U VPX
Model 5690 AMC • Model 7690 PCI • Model 7290 6U cPCI • Model 7390 3U cPCI •

Model 7190 PMC

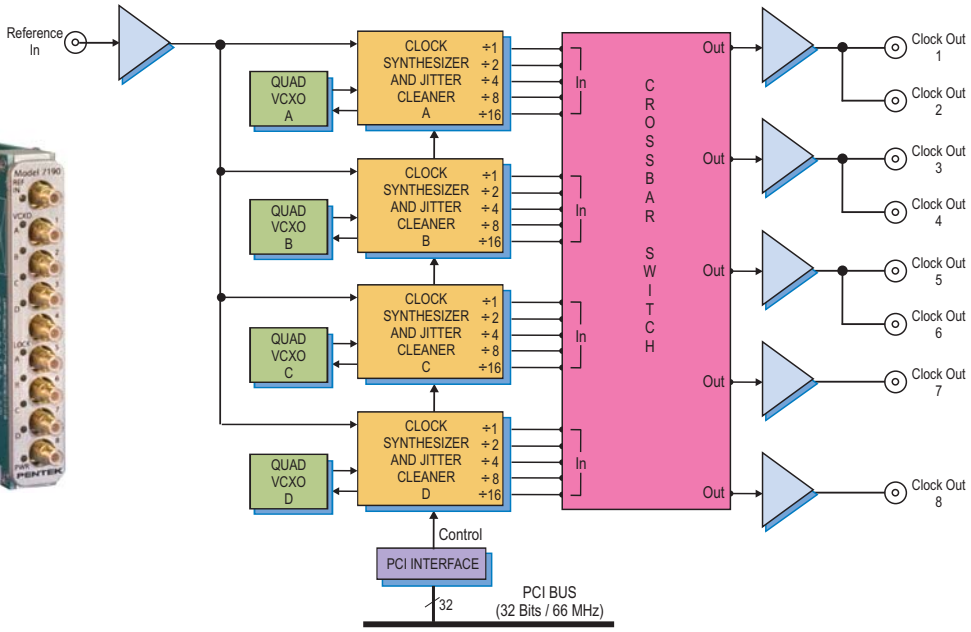


Figure 65

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs and can be phase-locked to an external reference signal.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 MHz and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7190 are also available as a PCIe half-length board (Model 7890), 3U VPX board (Model 5390), 6U VPX (Models 5790 and 5890 with dual density), AMC (Model 5690) PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).

Programmable Multifrequency Clock Synthesizer

Model 7191 PMC • Model 7891 PCIe • Model 5391 3U VPX • Models 5791, 5891 6U VPX
Model 5691 AMC • Model 7691 PCI • Model 7291 6U cPCI • Model 7391 3U cPCI

Model 7191 PMC

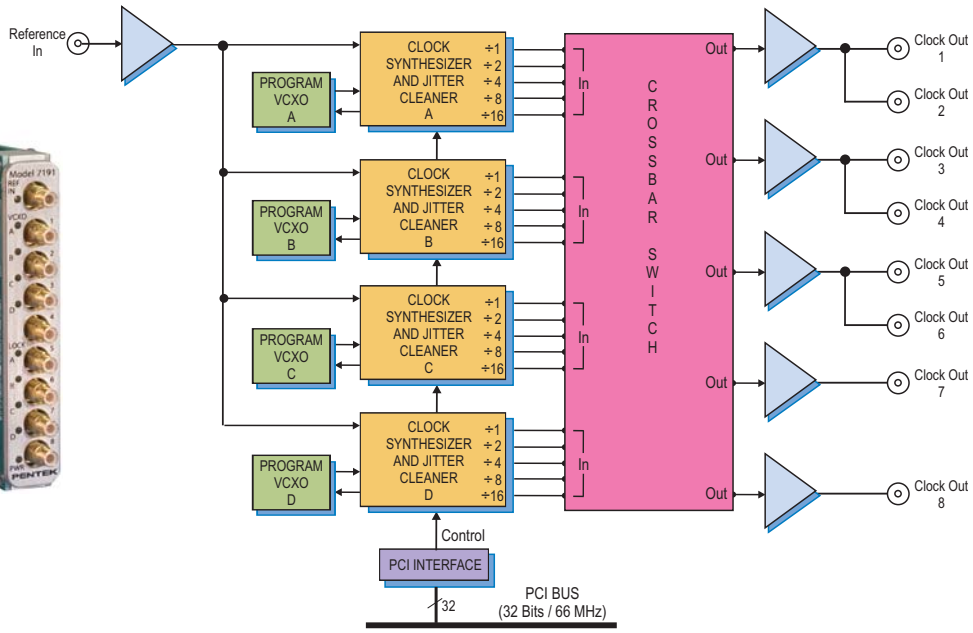


Figure 66

Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7191 are also available as a PCIe half-length board (Model 7891), 3U VPX board (Model 5391), 6U VPX (Models 5791 and 5891 with dual density),AMC (Model 5691), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).

High-Speed Synchronizer and Distribution Board

Model 7192 PMC/XMC • Model 7892 PCIe • Model 5292 3U VPX • Models 5792, 5892 6U VPX
Model 5692 AMC • Model 7292 6U cPCI • Model 7392 3U cPCI • Model 7492 6U cPCI

Model 7192 PMC/XMC

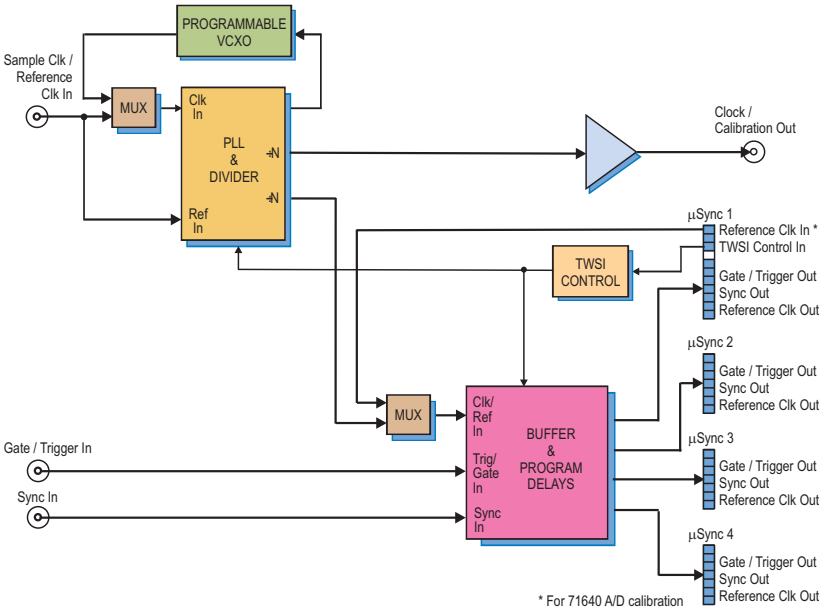


Figure 67

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

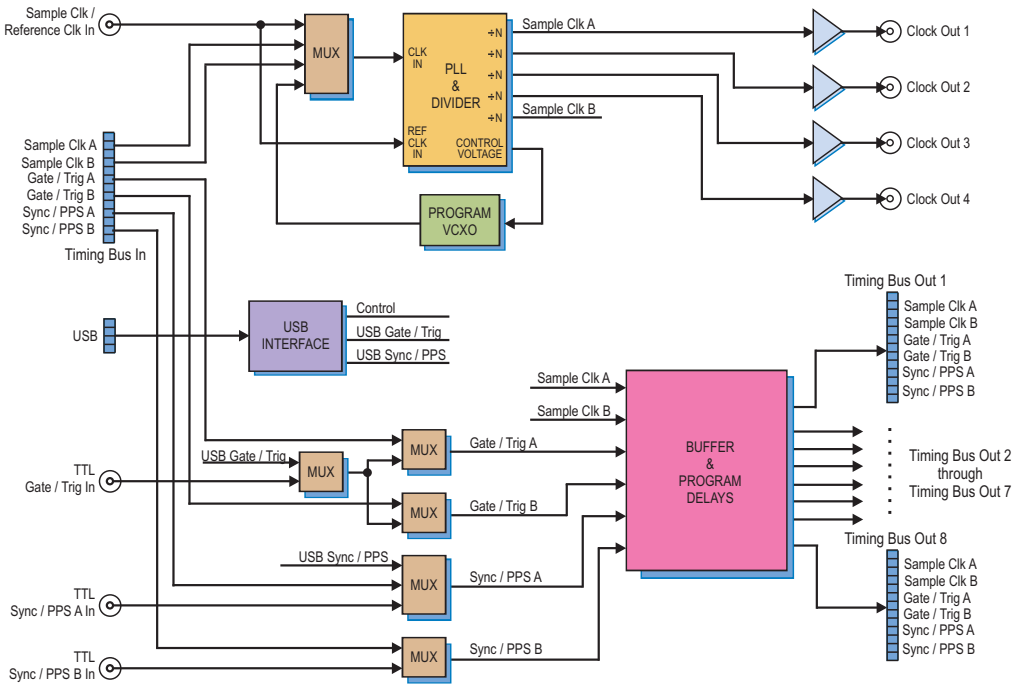
The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt and Onyx families including the 71630/71730 1 GHz A/D and D/A XMC, the 71640/71741 3.6 GHz A/D XMC and the 71670/71771 Four-channel 1.25 GHz, 16-bit D/A XMC.

Versions of the 7192 are also available as a PCIe half-length board (Model 7892), 3U VPX (Model 5292), 6U VPX (Models 5792 and 5892 with dual density), AMC (Model 5692), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).

System Synchronizer and Distribution Board

Model 7893 - Half-length PCIe



Model 7893
PCIe

Figure 68

Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and all complementary models in the Onyx family.

High-Speed Clock Generator

Model 7194 PMC/XMC • Model 7894 PCIe • Model 5294 3U VPX • Models 5794, 5894 6U VPX Model 5694 AMC • Model 7294 6U cPCI • Model 7394 3U cPCI • Model 7492 6U cPCI

Model 7194 PMC/XMC

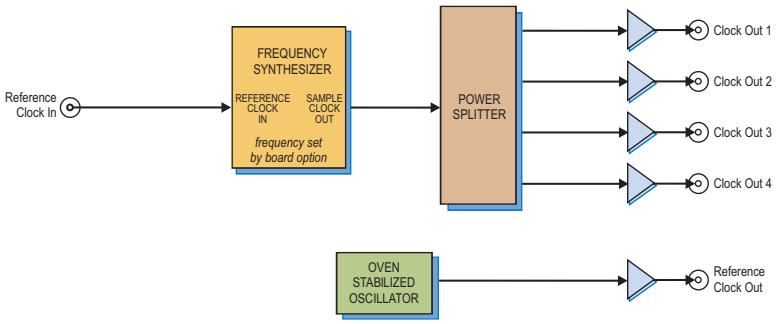


Figure 69

Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

The Model 7194 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power. The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Versions of the 7194 are also available as a PCIe half-length board (Model 7894), 3U VPX (Model 5294), 6U VPX (Models 5794 and 5894 with dual density), AMC (Model 5694), 6U cPCI (Models 7294 and 7494 dual density), and 3U cPCI (Model 7394).

High-Speed System Synchronizer Unit

Model 9192 - Rackmount

Model 9192

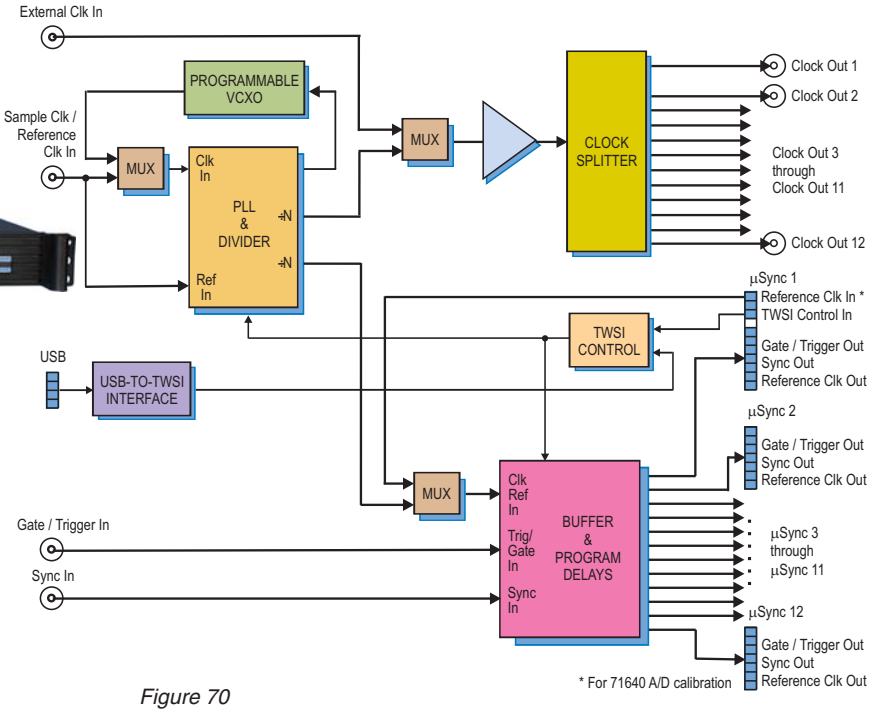


Figure 70

Model 9192 Rack-mount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71741 3.6 GHz A/D modules and provides a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 also supports high-speed models in the Onyx family.

Talon High-Speed Recording Systems: Flexible and Deployable Solutions

High-Speed Recording Systems

Talon® High-Speed Recording Systems eliminate the time and risk associated with new technology system development. With increasing pressure in both the defense and commercial arenas to get to the market first, today's system engineers are looking for more complete off-the-shelf system offerings.

Out of the box, these systems arrive complete with a full-featured virtual operator control panel ready for immediate data recording and/or playback operation.

Because they consist of modular COTS board-level products and the flexible Pentek SystemFlow® software, they are easily scalable to larger multichannel data acquisition and recording applications requiring aggregate recording rates of up to 5.0 GB/sec.

Ready-to-Run Recording Systems

Depending on model, the Pentek offerings are fully integrated systems featuring a range of A/D and D/A resources or digital I/O with high-speed disk arrays.

Since these systems are built on a Windows workstation, users can easily install post-processing and analysis tools to operate on the recorded data.

Pentek systems provide a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels of up to 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

TALON RTV VALUE RECORDER

RTV Recording Systems are excellent value for under $20,000

TALON RTS COMMERCIAL RECORDER

RTS Recording Systems are designed for commercial applications

TALON RTR RUGGED RECORDER

RTR Recording Systems are designed for harsh environments

TALON RTX EXTREME RECORDER

RTX Recording Systems are designed for extreme environments

ANALOG RECORDERS

Click Here for the SYSTEM SELECTOR

DIGITAL RECORDERS

Click Here for the SYSTEM SELECTOR

Recording Systems Form Factors

Pentek's High-Speed Recording Systems are available as Lab Systems, Portable Systems, Rugged, and Extreme Systems.

RTV and RTS Lab Systems are housed in a 19-in. rack-mountable chassis in a PC server configuration. They are designed for commercial applications in a lab or office environment.

RTS Lab system

RTR Portable Systems are available in a small briefcase-sized enclosures with integral LCD display and keyboard. They, too, provide a PC server configuration and are designed for harsh environment field applications where size and weight is of paramount importance.

RTR Portable System

RTR Rugged Rackmount Systems are housed in a 19-in. rugged rack-mountable chassis. They are built to survive shock and vibration and they target operation in harsh environments and remote locations that may be unsuitable for humans.

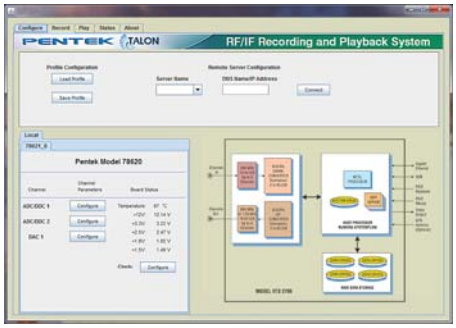
RTR Rackmount system

RTX Extreme Systems are available in either a rackmount chassis designed to military specs, or a ½ ATR chassis. They are designed to operate under extreme environmental conditions using forced-air or conduction-cooling to draw heat from system components.

RTX Rackmount system

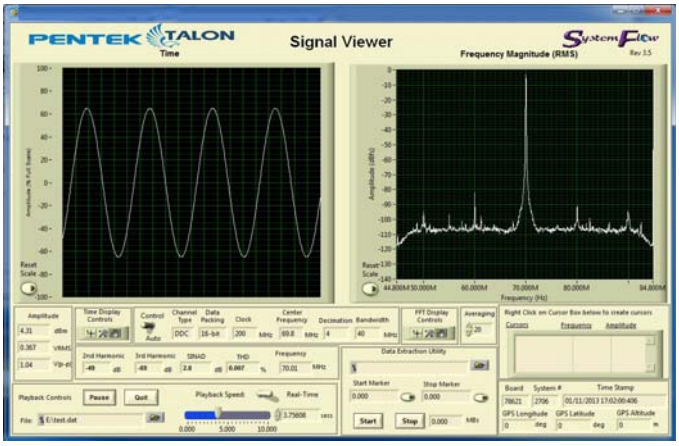
½ ATR system

Pentek SystemFlow Recording Software for Analog Recorders



Recorder Interface

Hardware Configuration



Signal Viewer

Figure 71

The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek analog high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

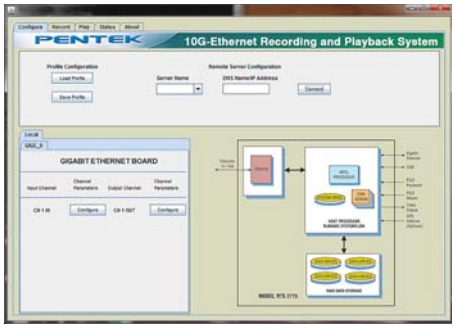
The **Recorder Interface** shows a system block diagram and includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The **Hardware Configuration** screen provides a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

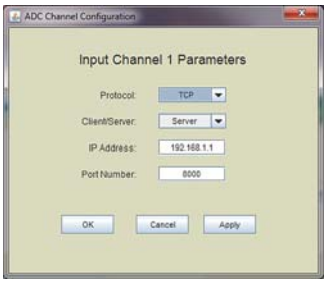
The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

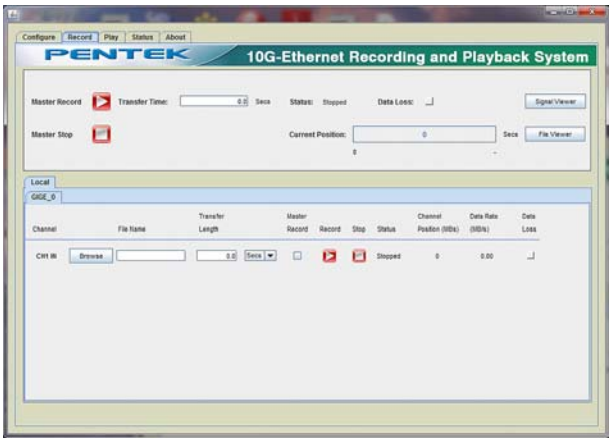
Pentek SystemFlow Recording Software for Digital Recorders



Main Interface



Hardware Configuration



Record Screen

Figure 72

The SystemFlow **Main Interface** for Digital Recorders shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream.

The **Configure** screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The **Record** screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk- full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.

200 MS/sec RF/IF Rackmount Value Recorder

Model RTV 2601

Model RTV 2601

TALON RTV VALUE RECORDER

SystemFlow

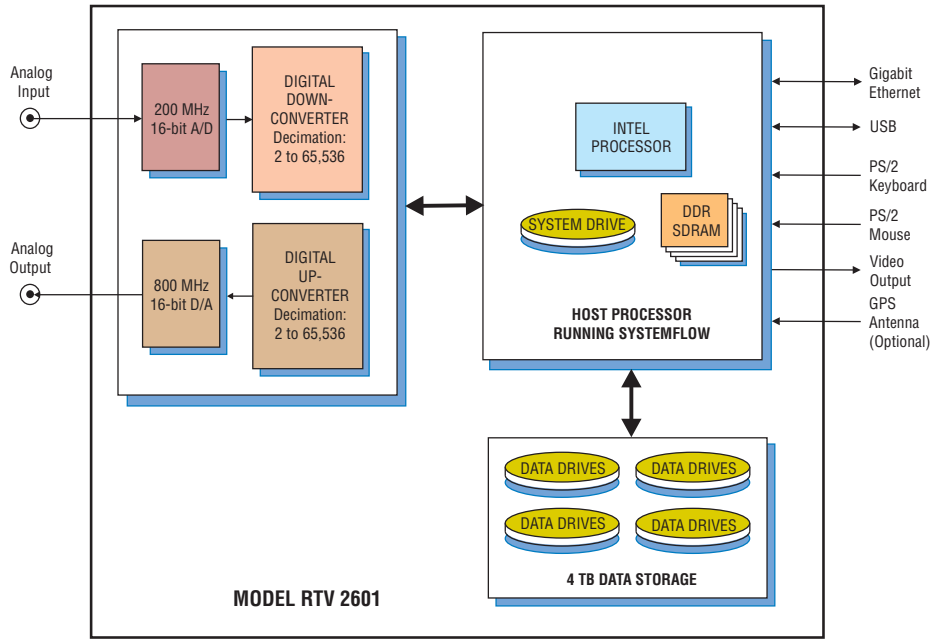


Figure 73

The Talon RTV 2601 is a turnkey multiband recording and playback system used for recording and reproducing signals with bandwidths up to 80 MHz. The RTV 2601 uses a 16-bit, 200 MHz A/D converter to provide real-time sustained recording rates to disk of up to 400 MB/sec. The A/D is complemented with a 16-bit 800 MHz D/A that provides the ability to reproduce signals captured in the field.

The RTV 2601 comes in a 4U 19 in. rackmount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available at the front. Air is pulled through the system from front to back allowing it to operate at ambient temperatures from 5 to 35 deg C.

The RTV 2601 includes a programmable digital downconverter so users can configure the system to capture signals with frequencies as low as 300 kHz and as high as 700 MHz. Corresponding signal bandwidths range from a few kilohertz to 80 MHz. A digital upconverter and D/A produce an analog output matching the recorded IF signal frequency.

The system includes a built-in sample clock synthesizer programmable to any desired frequency from 10 MHz to 200 MHz. This clock synthesizer can be locked to an external 10 MHz reference clock and has excellent phase noise characteristics. Alternately, the user can supply an external sample clock to drive the A/D and D/A converters. The RTV 2601 also supports external triggering, allowing users to trigger a recording or playback on an external signal.

The RTV 2601 includes the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. As an option, a GPS or IRIG receiver card can be supplied with the system for accurate time stamping of recorded data.

Serial FPDP Rackmount Value Recorder

Model RTV 2602

Model RTV 2602

TALON RTV VALUE RECORDER

SystemFlow

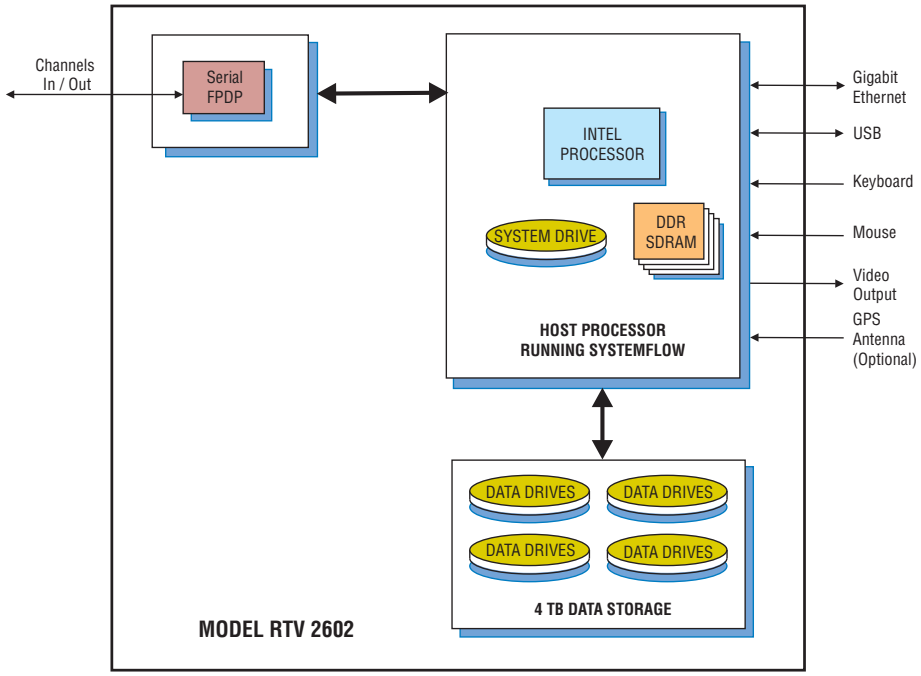


Figure 74

The Talon RTV 2602 Serial FPDP Value Recorder is designed to provide a low-cost solution to users looking to capture and play back multiple Serial FPDP streams. It can record up to four Serial FPDP channels to the built-in 4 TB RAID consisting of cost-effective, enterprise-class HDD storage. It is a complete turnkey recording system, ideal for capturing any type of streaming sources. These include live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification.

The RTV 2602 comes in a 4U 19 in. rack-mount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available in the front. Air is pulled through the system from front to back to allow operation at ambient temperatures from 5° to 35° C.

The RTV 2606 can be populated with up to four SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates. Up to four channels can be recorded simultaneously with an aggregate recording rate of up to 400 MB/sec.

As an option, a GPS or IRIG receiver card can be supplied with the system providing accurate time stamping of recorded data. Additionally, the GPS receiver delivers GPS position information that can be recorded along with the input signals.

The RTV 2602 includes the Pentek SystemFlow recording software which features a Windows-based GUI.

200 MS/sec RF/IF Rugged Portable Recorder

Model RTR 2726A Rugged Portable • Model RTS 2706 Rackmount Lab • Model RTR 2746 Rugged Rackmount • Model RTX 2766 Extreme Rackmount • Model RTX 2786 ½ ATR

Model RTR 2726A

TALON RTS COMMERCIAL RECORDER

SystemFlow

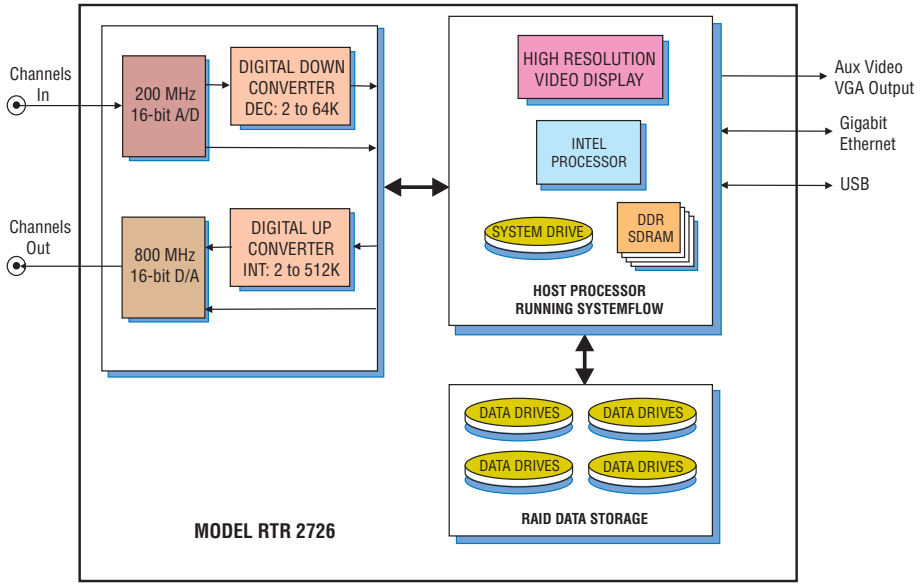


Figure 75

The Talon RTR 2726A is a turnkey, multiband recording and playback system that allows the user to record and reproduce high-bandwidth signals with lightweight, portable and rugged packages. This model provides aggregate recording rates of up to 3.2 GB/sec and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726A is supplied in a small footprint portable package measuring only 16.0" W x 6.9" D x 13.0" H and weighing just less than 30 pounds.

With measurements similar to small briefcases, this portable workstation includes Intel Core i7 processors, high-resolution 17" LCD monitors, and up to 15.3 TB of SSD storage.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, that provide fully-programmable systems capable of recording and reproducing a wide range of signals.

Included with this system is Pentek's SystemFlow recording software. Built on a Windows 7 Professional workstation with high performance Intel Core i7 processor, the system allows the user to install post-processing and analysis tools to operate on the recorded data. They record data to the native NTFS file system, providing immediate access to the data. Custom configurations can be stored as profiles and later loaded when needed, so users can select preconfigured settings with a single click.

Versions of the RTR 2726A are also available as a Rackmount Lab unit (Model RTS 2706), Rugged Rackmount (Model RTR 2746), Extreme Rackmount (Model RTX 2766) and Extreme ½ ATR (Model RTX 2786)

500 MS/sec RF/IF Rackmount Lab Recorder

Model RTS 2707 Rackmount Lab • Model RTR 2727 Rugged Portable
Model RTR 2747 Rugged Rackmount • Model RTX 2767 Extreme Rackmount

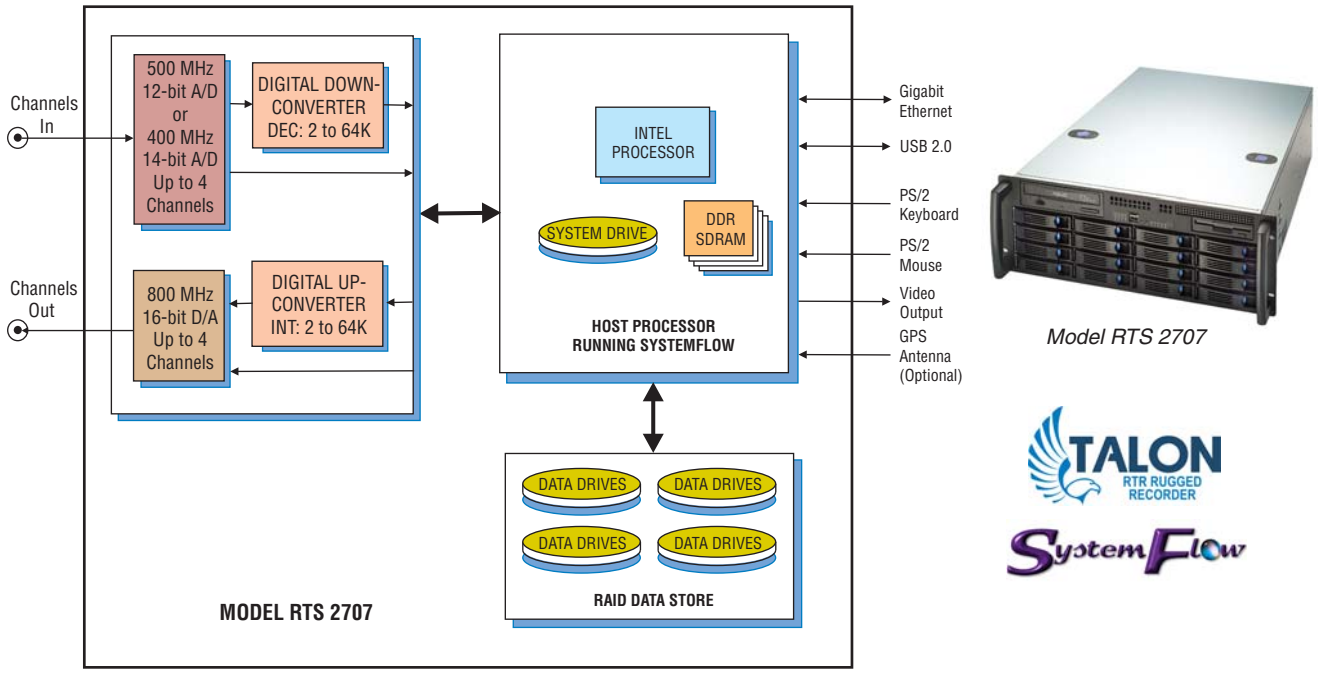


Figure 76

The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides agregate recording rates up to 1.6 GB/sec.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals. Optional GPS time and position stamping allows the user to record this critical signal information.

The RTS 2707 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder.

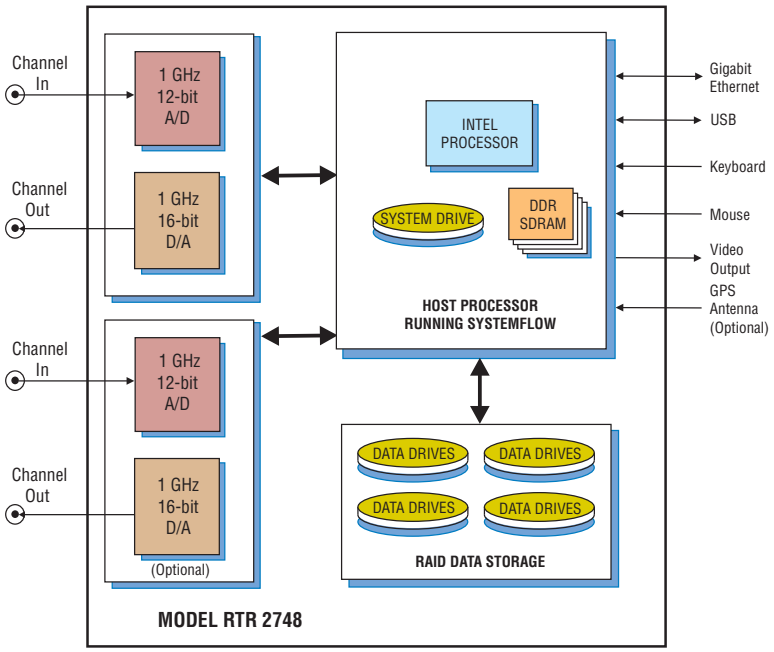
The RTS 2707 is configured in a 4U 19" rackmountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

Versions of the RTS 2707 are available as Rugged Portable (Model RTR 2727), Rugged Rackmount (Model RTR 2747), and Extreme Rackmount (Model RTX 2767).

1 GS/sec RF/IF Rugged Rackmount Recorder

Model RTR 2748 Rugged Rackmount • Model RTR 2728 Rugged Portable
Model RTX 2768 Extreme Rackmount



Model RTR 2748

Figure 77

The Talon RTR 2748 is a turnkey recording and playback system that allows users to record and reproduce signals with bandwidths up to 500 MHz. The RTR 2748 can be configured as a one- or two-channel system to provide real-time aggregate recording and playback rates up to 4.0 GB/sec to an array of solid-state drives.

The RTR 2748 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converters. A built-in synchronization module is provided to allow for multi-channel phase-coherent operation. GPS time and position stamping is optionally available.

The RTR 2748 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2748 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2748 records data to the native NTFS file system that provides immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet ports, or USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2748 performs well in ground, ship-borne and airborne environments. The drives can be easily removed or exchanged during a mission to retrieve the data.

Versions of the RTR 2748 are also available as a Rugged Portable (Model RTR 2728), and Extreme Rackmount (Model RTX 2768).

3.6 GS/sec Ultra Wideband RF/IF Extreme Rackmount Recorder

Model RTX 2769 Extreme Rackmount • Model RTR 2729A Rugged Portable
Model RTR 2749 Rugged Rackmount

Model RTX 2769

TALON RTX EXTREME RECORDER

SystemFlow

QuickPac Compatible

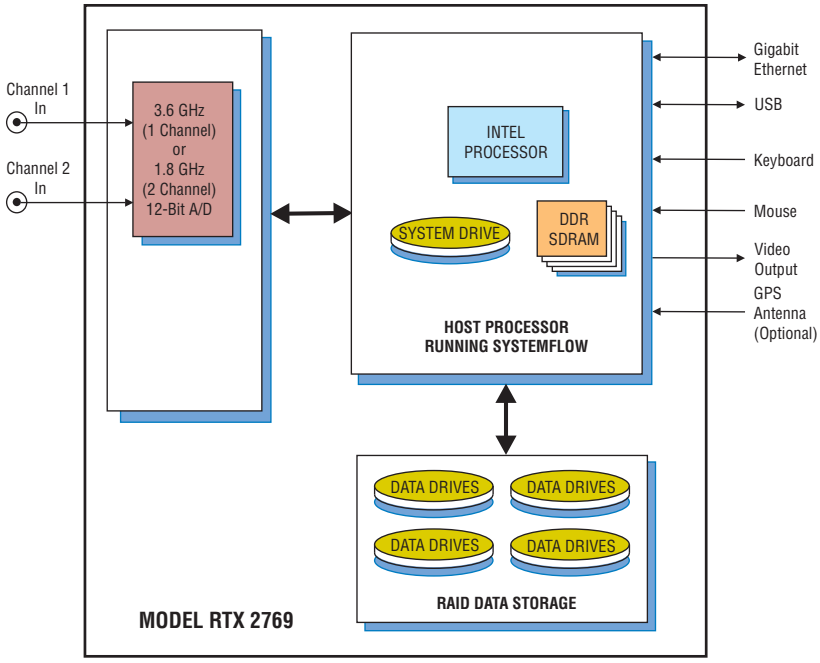


Figure 78

The Talon RTX 2769 is a turnkey system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2769 is intended for military, airborne and UAV applications requiring a rugged system.

Aimed at recording high-bandwidth signals, the RTX 2769 uses 12-bit, 3.6 GHz A/D converters. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit- or 16-bit-wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word). A high-speed RAID array provides an aggregate streaming recording rate to disk of 4.8 GB/sec.

The RTX 2769 uses Pentek's high-powered Virtex-7-based Onyx boards that provide the data streaming engine for the high-speed A/D converters. Channel and packing modes as well as gate and trigger settings are among the selectable system parameters, providing complete control over this ultra wideband recording system.

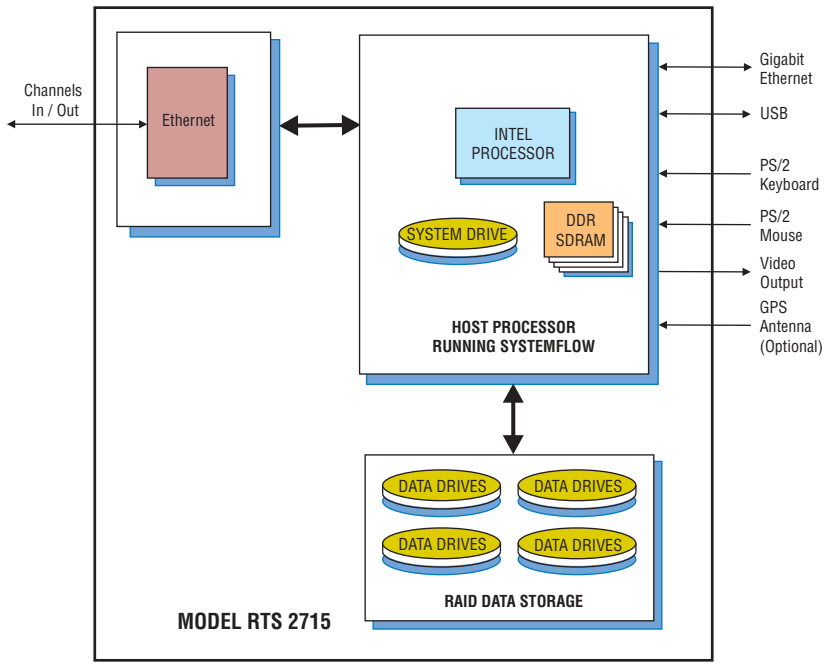
Built on a Windows 7 Professional workstation, the RTX 2769 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2769 records data to the native NTFS file system that provides immediate access to the recorded data.

The Talon RTX 2769 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the RTX 2769 are available as a Rugged Portable (Model RTR 2729A), and Rugged Rackmount (Model RTR 2749).

10-Gigabit Ethernet Rackmount Recorder

Model RTS 2715 Rackmount Lab • Model RTR 2755 Rugged Rackmount
Model RTX 2775 Extreme Rackmount



Model RTS 2715

TALON RTS COMMERCIAL RECORDER

SystemFlow

Figure 79

The Talon RTS 2715 is a turnkey rackmount lab recording system for storing one or two 10-gigabit Ethernet (10GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Versions of the RTS 2715 are also available as Rugged Rackmount (Model RTR 2755), and Extreme Rackmount (Model RTX 2775).

Serial FPDP Rugged Portable Recorder

Model RTR 2736A Rugged Portable • Model RTS 2716 Rackmount Lab
Model RTR 2756 Rugged Rackmount • Model RTX 2776 Extreme Rackmount

Model RTR 2736A

TALON RTR RUGGED RECORDER

SystemFlow

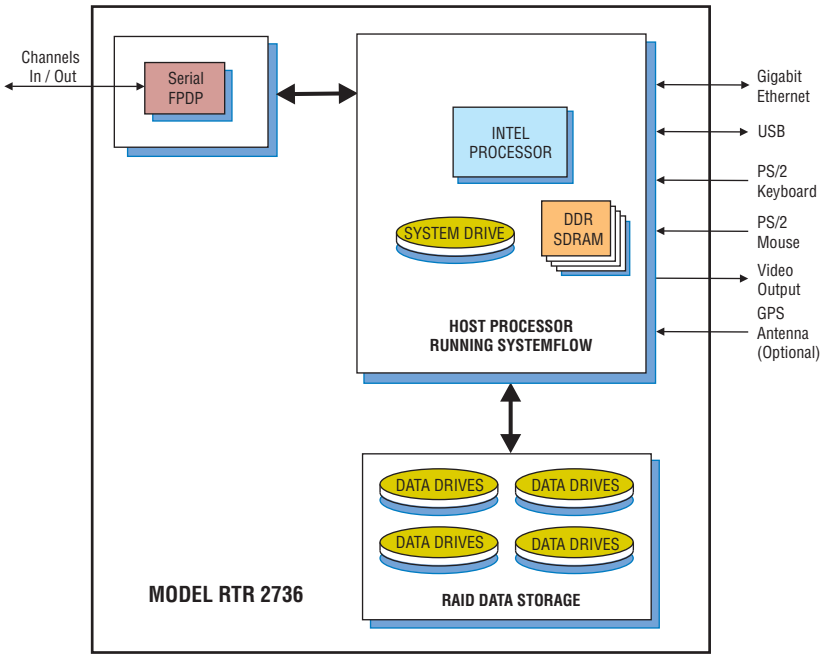


Figure 80

The Talon RTR 2736A is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, this system achieves aggregate recording rates up to 3.2 GB/sec.

The system can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per serial FPDP link.

The system includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736A is configured in portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built in extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and impact-resistant protective glass. Using vibration- and shock-resistant SSDs, the system is designed to operate reliably as a portable field system in harsh environments.

Versions of the RTR 2736A are also available as a Rackmount Lab unit (Model RTS 2716), Rugged Rackmount (Model RTR 2756), and Extreme Rackmount (Model RTX 2776).

LVDS Digital I/O Extreme Rackmount Recorder

Model RTX 2778 Extreme Rackmount • Model RTS 2718 Rackmount Lab
Model RTR 2738 Rugged Portable • Model RTR 2758 Rugged Rackmount

Model RTX 2778

TALON RTX EXTREME RECORDER

SystemFlow

QuickPac Compatible

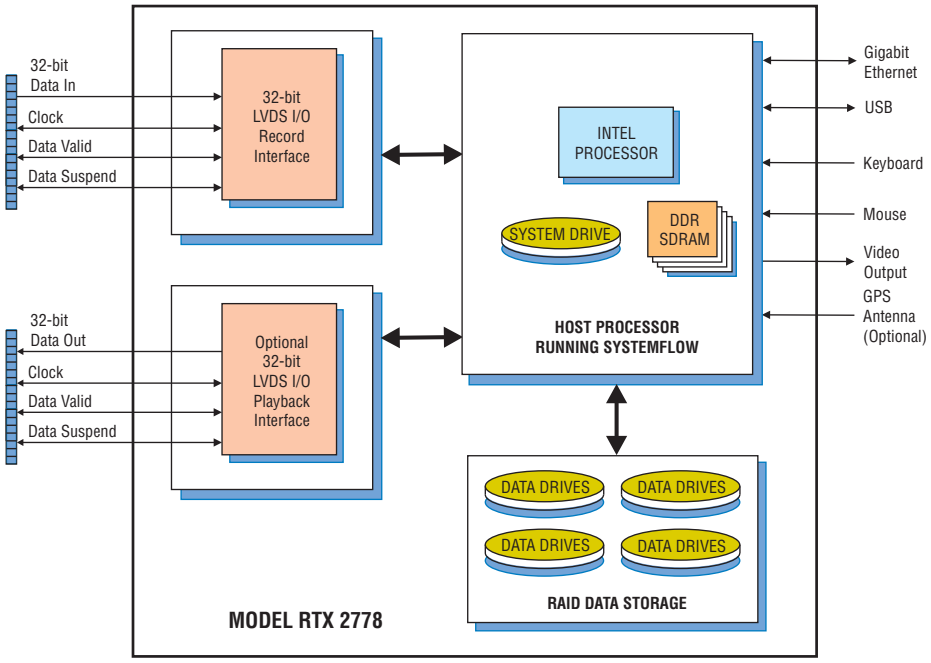


Figure 81

The Talon RTX 2778 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2778 is intended for military, airborne and UAV applications requiring a rugged system.

The RTX 2778 records and plays back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves aggregate recording rates of up to 1.0 GB/sec.

The RTX 2778 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

The RTX 2778 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Built on a Windows 7 Professional workstation, the RTX 2778 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2778 records data to the native NTFS file system, providing immediate access to the recorded data.

The Talon RTX 2778 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the RTX 2778 are also available as a Rackmount Lab unit (Model RTS 2718), Rugged Portable (Model RTR 2738), and Rugged Rackmount (Model RTR 2758).

64-Channel Software Radio Recording System

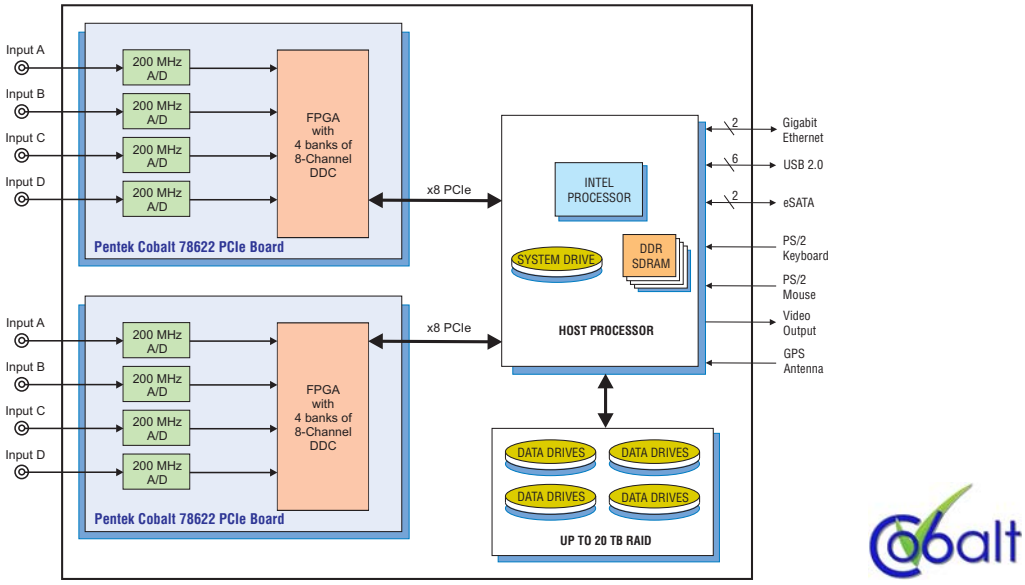


Figure 82

Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the eight channels within each bank share a common decimation setting that can range from 16 to 8192. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An onboard clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel Core i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

L-Band Signal Processing System

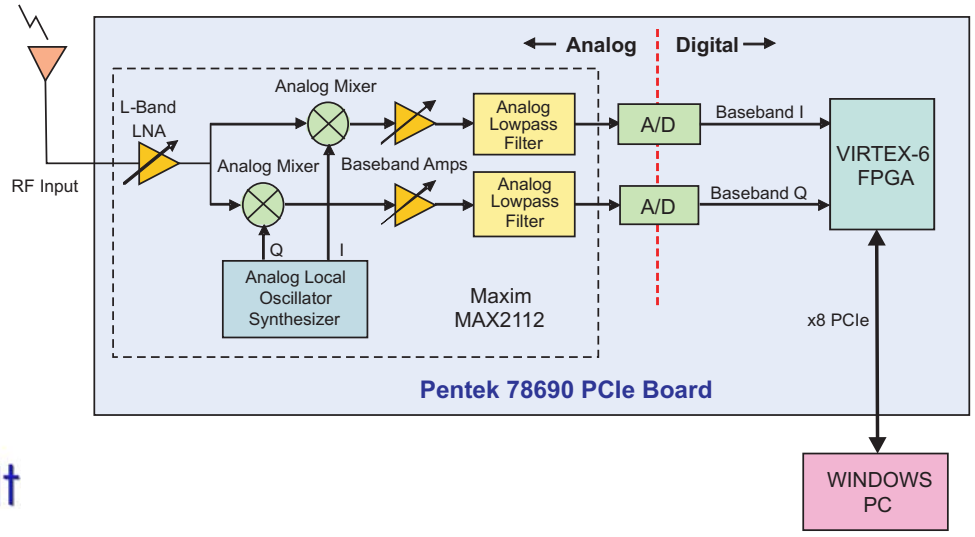


Figure 83

The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz . The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size adderesses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.

8-Channel OpenVPX Beamforming System

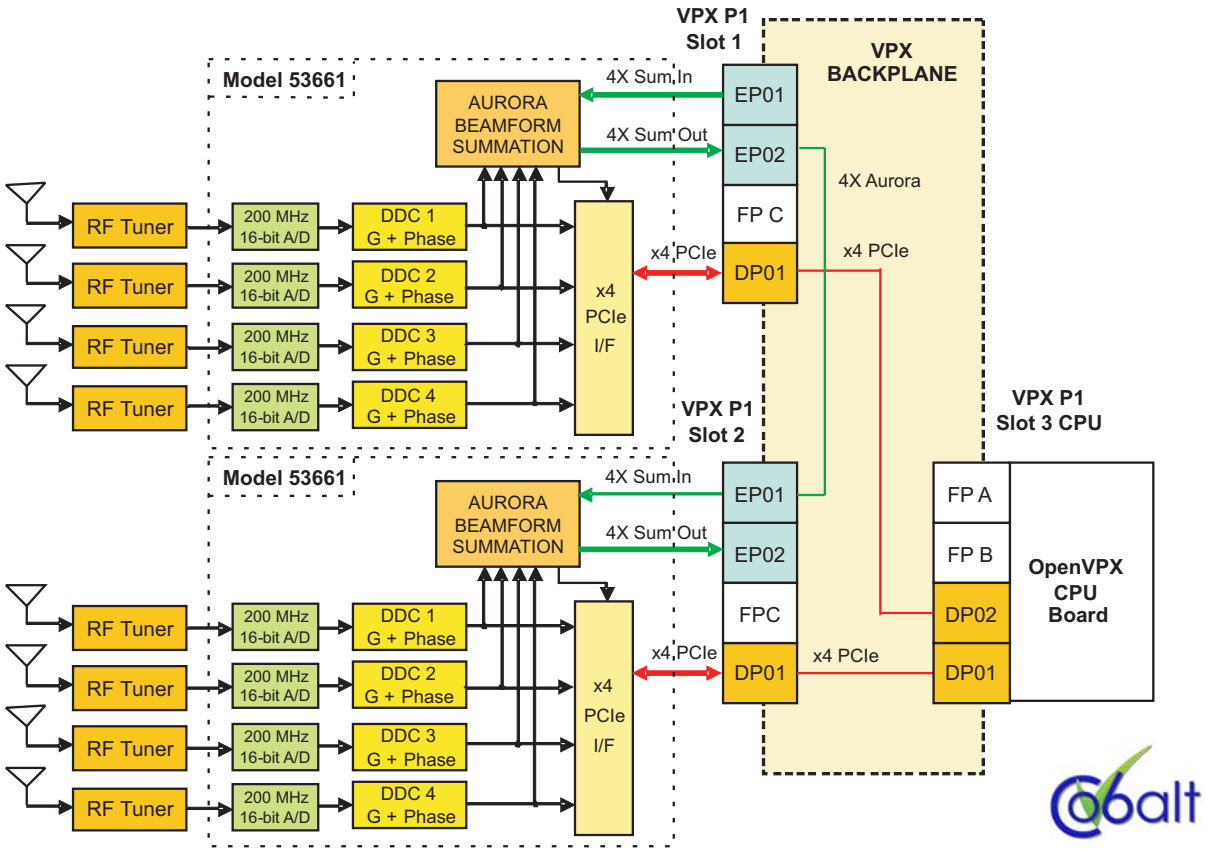


Figure 84

Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

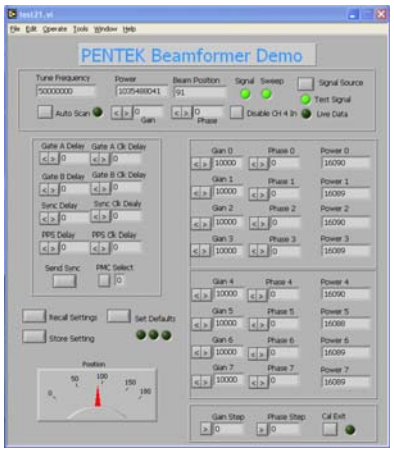
The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX "fat pipes".

The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

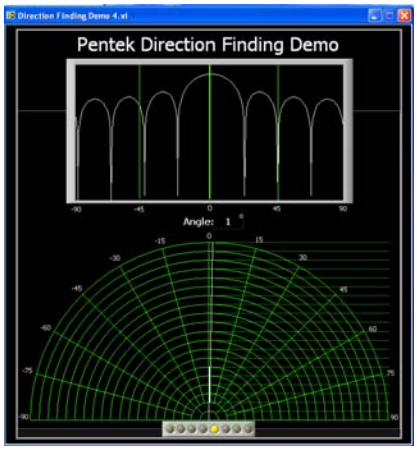
Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. ➤

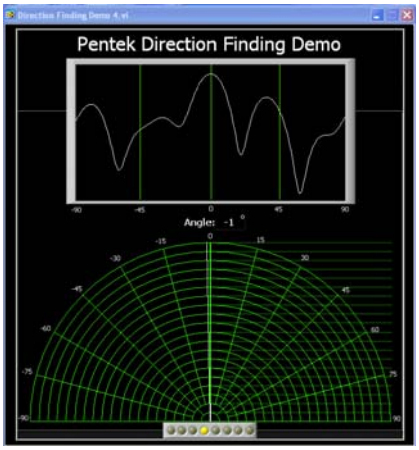
8-Channel OpenVPX Beamforming Demo system



Beamforming Demo Control Panel



Theoretical 7-lobe Beamforming Patern



Real-Life Beamforming Patern

Figure 85

➤ Beamforming Demo System

The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum sensitivity across arrival angles from -90^{O} to +90^{O} perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0^{O} angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link:
Beamforming Demo.